

# An 8-bit 800- $\mu$ W 1.23-MS/s Successive Approximation ADC in SOI CMOS

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**Abstract**—We report on an 8-bit successive approximation analog-to-digital converter (SA-ADC) that was designed and fabricated in 0.5- $\mu$ m silicon on sapphire CMOS technology. The SA-ADC is capable of 32-MHz operation, providing 1.23-MS/s conversion rates, and consumes 800  $\mu$ W at 3.3-V supply. The lack of substrate parasitic capacitances enables the use of small-area capacitors and reduces the noise coupling to the analog nodes. The circuits employ MOS transistors of different thresholds to optimize the performance and power dissipation of the system.

**Index Terms**—Analog-to-digital converters (ADCs), low power, low voltage, silicon-on-insulator (SOI), silicon-on-sapphire (SOS), successive approximation (SA).

## I. INTRODUCTION

SUCCESSIVE approximation analog-to-digital converters (SA-ADCs) are capable of low-power operation, have a small footprint, and can deliver 8–10-bit resolution [1]–[3]. SA-ADCs are ideal for low-power applications and the average conversion performance necessary in data acquisition for systems on a chip (SOC), column-parallel architecture for imagers, and sensor networks. In recent years, the proliferation of wireless sensors has intensified the design of ultralow-power sensor interfaces, with the ADC being a common component. The limited power constrained by the use of battery-operated and energy-harvesting devices has in particular led to the design of algorithmic ADCs that are operating with energy levels close to the theoretical minimum [4], [11].

We report on the design of an 8-bit SA-ADC in a 0.5- $\mu$ m silicon-on-sapphire (SOS) CMOS technology (Fig. 1). The absence of parasitics and the isolated substrate in the SOS CMOS process can decrease the noise levels and the power consumption of analog ADCs [5], [6]. Our ADC circuit design employs a split-capacitor array that can provide high-precision conversions while using one eighth of the area used by standard SA-ADCs. We use transistors of different thresholds to optimize the performance of the digital and analog circuits to provide both low power and also high conversion speeds. In this paper, by means of our initial prototype, we provide evidence of the advantages of silicon-on-insulator (SOI) design of high-performance analog circuit interfaces.

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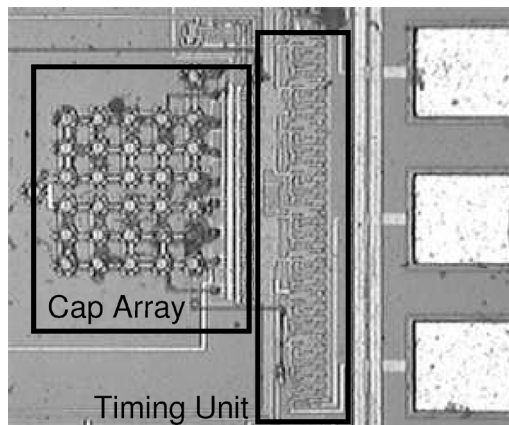


Fig. 1. Micrograph of the fabricated ADC core.

## II. ADC OPERATION

The capacitive ladder is the basic structure of the SA-ADC. It implements a charge scaling digital-to-analog converter (DAC), which algorithmically minimizes the error between its output voltage and the analog input to be converted [7], [8]. In our implementation, we use a less conventional split-capacitor array reported in Fig. 2. A conversion begins with a global reset that discharges all of the capacitors in the array and the SA register cells. The input signal  $V_i$  ( $V_i < V_{\text{ref}}$ ) is then sampled by strobing the signal  $fs$ . The algorithmic conversion begins by adding  $V_{\text{ref}}/2$  to  $V_i$  and comparing the value with  $V_{\text{ref}}$ . If the value is larger, the corresponding capacitor is reset and its register is cleared. If the value is smaller, the MSB will be set to a logical one. The algorithm repeats  $N = 8$  (b) times, and the voltage on the upper plates of the capacitor array converges to the input value  $V_i$

$$V_{\text{DAC}} = \sum_{k=0}^{N-1} D_k 2^{k-N} V_{\text{ref}}. \quad (1)$$

Equation (1) represents the voltage  $V_{\text{DAC}}$  in Fig. 2. This value is compared with the reference voltage  $V_{\text{ref}}$  at each iteration.  $D_k$  is the digital output value of the  $k$ th SA register cells [8]. Fig. 3 shows the waveforms of the signals required for the ADC operation in Fig. 2.

## III. SOS ADVANTAGE

The precision of an SA-ADC is proportional to the accuracy of its capacitors and the coupling of substrate noise. Using the SOS technology, we can reduce the size of the capacitor array without compromising performance. In fact, capacitors

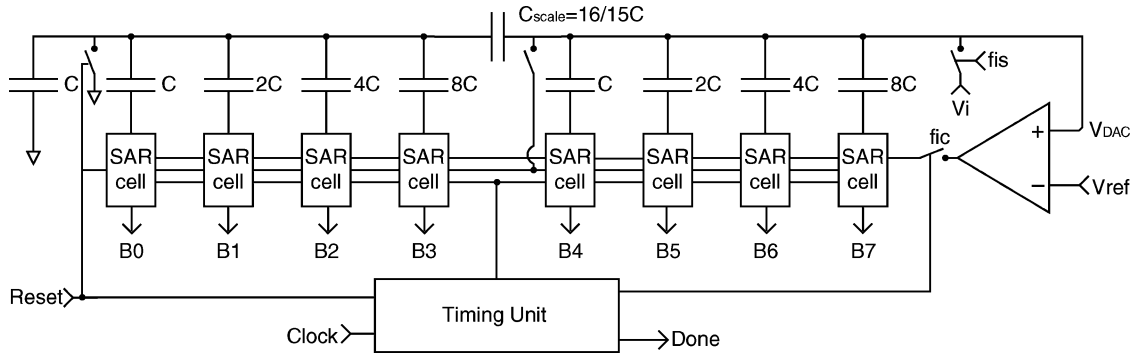


Fig. 2. Split-capacitor array and successive approximation register.

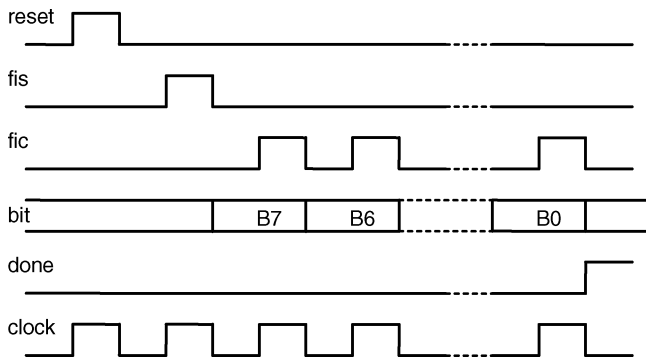


Fig. 3. Waveforms of the signals required for the ADC operation in Fig. 2.

fabricated in bulk CMOS technologies have substrate parasitic capacitance that is proportional to their area. This parasitic capacitance can couple noise from the substrate and limit the reduction of unit capacitors due to matching. In contrast, capacitors fabricated in SOI technologies, and in particular SOS, virtually eliminate parasitic capacitances. As an example, a 100-fF Poly-Poly2 linear capacitor in a regular CMOS 0.5- $\mu$ m process has a parasitic capacitance to the substrate of 9.5 fF (extracted). The same 100-fF capacitor in SOS has a parasitic capacitance of 65 aF. In addition, by using the split-capacitor array of Fig. 2, the area of SOS capacitor arrays can be one eighth of the ones fabricated in bulk CMOS technologies while maintaining the specified accuracy. In our split-capacitor array, we use 31 capacitors as opposed to the 256 needed for a full array! With a reduced array size, the ADC circuits consume less power as less energy is wasted in charging and discharging larger arrays and the parasitic charge-sharing nodes. This way, the lower bound on power consumption of the ADC is limited only by the power used in the comparator.

Note that, in an SA-ADC, capacitor matching limits the minimum size of usable capacitors. In the SOS, MIM-type capacitors have a standard deviation of approximately 50% at a nominal value of 5 fF [6], [9]. This value is the lower bound on usable capacitors due to matching in the 0.5- $\mu$ m process. Notice also that capacitor switching noise ( $kT/C$ ) does not impose a limitation for an 8-bit ADC with a  $V_{ref}$  of 1 V. In fact,  $kT/C$  noise in a 5-fF capacitor is less than 1 mV, while the LSB value is 4 mV. Therefore, it is theoretically possible to obtain a 10-bit SA-ADC in SOS. In practice, the unit capacitor cannot be much

smaller than the gate capacitance of M1 or M2 in Fig. 4. Otherwise, the ADC input range will be reduced and the LSB value will also be reduced. In this design, we use a very conservative unit capacitance value of 100 fF to avoid nonlinear effects at the array-to-comparator interface in our first prototype.

The advantage of the use of SOI/SOS technologies is that the split-capacitor array architecture of Fig. 2 is obtainable without the complications of substrate parasitics. This architecture is very sensitive to any size error of the  $C_{scale}$  capacitor in Fig. 2. In standard bulk CMOS technologies, a truly floating coupling capacitor is not available, as one capacitor plate is facing the substrate, and thus accurate sizing is complicated and requires a very well-characterized process. The split-capacitor array can be obtained in the CMOS process as well, but it is complicated by the precise matching of the floating capacitor, since the substrate parasitics have to be taken into account. For this reason, the split-capacitor arrays is seldom used in standard CMOS [8]. In SOS instead, split-capacitor arrays are easily obtainable and do not require precise characterization.

#### IV. COMPARATOR DESIGN IN SOS

In our prototype, we used a standard high-speed comparator design [8], but innovate in the use of multiple threshold devices. The comparator (Fig. 4) uses an active load for fast switching. Zero-threshold MOS transistors are employed at the input stage (M1 and M2). Zero-threshold devices do not have a threshold adjustment implant and thus they are better matched compared to regular threshold devices. In addition, intrinsic-type transistors provide more transconductance. The load PMOS transistors M3–M6 are also of the intrinsic type. This provides better matching in the currents of the two branches of the differential amplifier, and the zero-threshold allows for operation close to the rail voltage. In addition, the active load provides high differential gain and a differential output for the next stage. The output of the comparator is a self biasing differential amplifier [8]. The digital output signal is strobed using the *outstrb* line (see the comparator strobe in Fig. 2), which activates the output only when a comparison is in process. Switches are all designed using regular threshold transistors.

The offset of the comparator was measured to be 15 mV with small M1 and M2 ( $W/L = 10/1 \mu\text{m}$ ) and has the effect of compressing the input voltage range. The comparator was optimized for speed and not power consumption. It is therefore inefficient

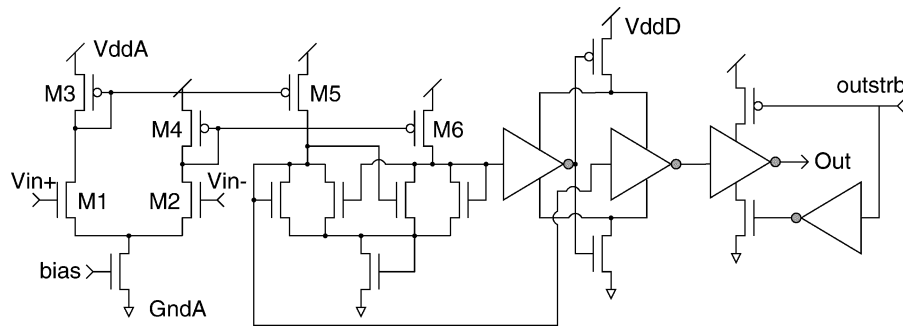


Fig. 4. Fast comparator circuit.

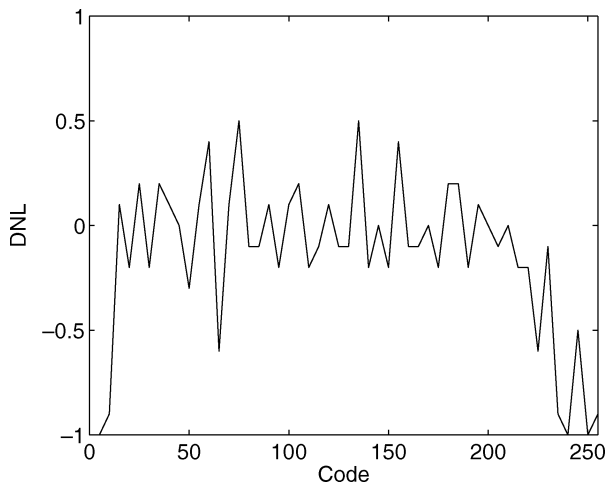


Fig. 5. ADC differential nonlinearity at 1 kHz.

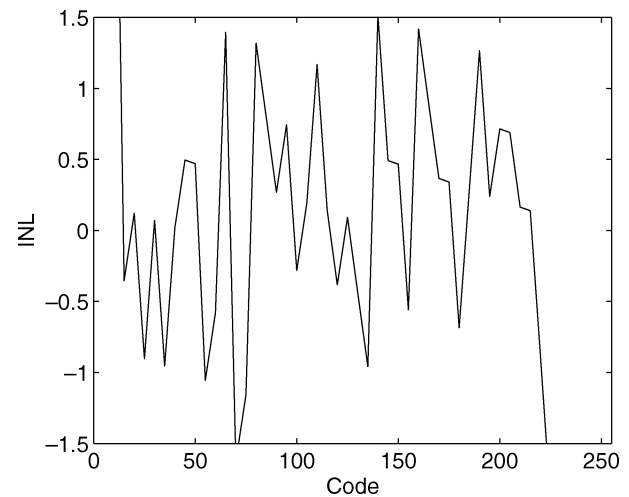


Fig. 6. ADC integral nonlinearity at 1 kHz.

at low conversion rates. We are targeting a low-power SOS comparator for our next generation of SA-ADCs.

## V. EXPERIMENTAL RESULTS

The SA-ADC occupies an area of  $450 \times 315 \mu\text{m}^2$  and operates with a power supply of 3.3 V. A micrograph of the core die is given in Fig. 1. The reference voltage  $V_{\text{ref}}$  was set to 2.7 V throughout testing. The power consumption of the chip is divided into analog and digital parts. The analog power supply provides currents for charging the capacitors, the DAC, and the comparator. The digital power supply provides current to the digital logic, clocking logic, and output buffers. The power dissipation of the analog circuits is 0.8 mW over the operational range of 1 kHz to 32 MHz. Digital power consumption accounts for 0.79 mW at 1-kHz operation and increases with the frequency because of the output buffers and capacitive load from the output pads (25 pF). The digital power consumption is almost completely due to driving the 8-bit parallel output and can be neglected if the output is used on-chip. In fact, the dynamic digital logic used in the control unit consumes  $38 \mu\text{W}$  at 3 V and running at 32 MHz (from simulations). A portion of the digital power consumption is used by the digital interface of the comparator. The following equation gives an empirical function for the digital power consumption  $P_d$ :

$$P_d = 0.78 + 1.2 \cdot 10^{-7} (f[\text{Hz}]) \quad [\text{mW}].$$

The circuit has been tested with clocks between 500 Hz to 32 MHz, which corresponds to a sampling frequency of 19 S/s–1.23 MS/s; one data conversion necessitates 26 clock cycles. The SA-ADC performed with an average of 0.18 LSB differential nonlinearity (DNL) and a mean integral nonlinearity (INL) of 0.87 LSB. Figs. 5 and 6 show plots of measured DNL and INL, respectively, as a function of the output digital code. The data were collected at a clock frequency of 1 kHz, corresponding to a sampling frequency of 38 S/s. The effective number of bits (ENOBs) for the data converter is eight for operational frequency of up to 3 MHz (115 kS/s) and with  $V_i = 2.01$  V. This number decreases to 7 b at a clock frequency of 10 MHz (384 kS/s). At faster speeds, the precision drops due to insufficient settling time for charging and discharging of the capacitor array as well as comparator settling time. The total harmonic distortion (THD) was measured sampling a 2-V peak-to-peak 1-kHz sine wave with a 1.38-MHz clock (53 KS/s). A plot of the measured fast Fourier transform (FFT) spectrum for the sampled 1-kHz waveform is given in Fig. 7. THD was measured to be  $-29.42$  dB. The spurious free dynamic range (SFDR) for the same input was measured to be 29.09 dB. The scaling capacitor  $C_{\text{scale}}$  in Fig. 2 introduces a scaling error that limits the harmonic-distortion performance of the ADC. The input signal range is 2.1 V (0.2–2.3 V) using a 3.3-V power supply with  $V_{\text{ref}}$  set to 2.7 V.

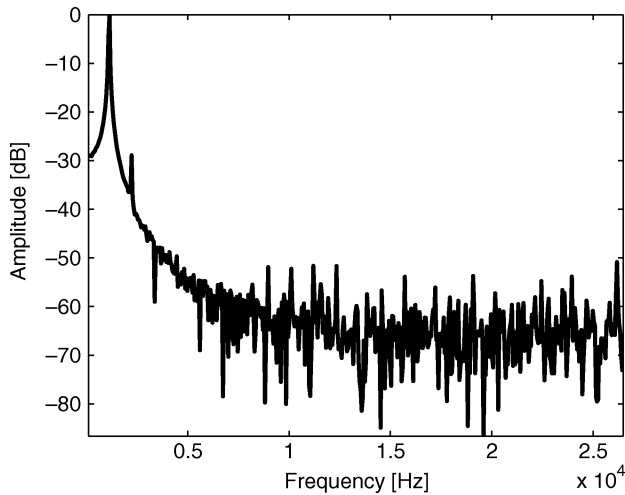


Fig. 7. Measured FFT spectrum for a 1-kHz sine waveform (2 Vpp) sampled at 53 KS/s.

TABLE I  
PERFORMANCE SUMMARY

Supply Voltage	3.3V
Digital Power	0.79mW @ 1KHz $0.78 + 1.2 \cdot 10^{-7} f(f[\text{Hz}])$ [mW]
Analog Power	0.77mW
Technology	0.5 $\mu$ m SOS ( $V_{tn} = 0.7\text{V}$ , $V_{tp} = -0.8\text{V}$ )
Operational Frequency	500Hz – 32MHz
Sampling Rate	19S/s – 1.23MS/s
Resolution	8 bits
Active Area	450x315 $\mu\text{m}^2$ , 916x790 $\mu\text{m}^2$ with pads
Input Range/Swing	2.1V (0.2 – 2.3V) on 3.3V supply
Unit Capacitor	100.6fF
Input Capacitance	3pF
DNL	0.18 LSB
INL	0.87 LSB
THD @ 1kHz	-31.48dB
SFDR @ 1kHz	31.65dB
ENOB @ 1kHz	7.92 bits

## VI. SUMMARY

A common figure of merit (FOM) used to compare ADC designs is given in [10]

$$\text{FOM} = \frac{2^{\text{ENOB}_{\text{DC}}} \cdot f_{\text{BW}}}{P_{\text{ADC}}} \quad (2)$$

The FOM value for the SOS ADC at 3.3-V operation is  $1.1 \cdot 10^{11}$  Hz/W, excluding the output pad drivers digital power. The

ADC can operate at a minimum of 1.5 V and a FOM of  $2.2 \cdot 10^{11}$  Hz/W. A summary of the ADC characteristics is given in Table I. The proposed SOS SA-ADC provides an 8-bit digital output, but effectively only 7 b are significant data, due to the low THD. The low THD and SFDR are due to the split-capacitor architecture and the use of a scaling capacitor. Our first SA-ADC prototype provides a sampling rate that is ten times higher than that of more recent ultralow-power SA-ADCs, and its FOM is approximately ten times worse [4], [11], [12]. The advantages of the use of SOI/SOS technology for the design of SA-ADCs is the reduction in parasitic capacitance in the capacitor array and its interconnect. This feature simplifies the design, thus eliminating the need for careful postlayout assessment of the parasitics and multiple design iteration that is typical of bulk CMOS.

In future design iteration, we plan to characterize the matching properties of the scaling capacitor of the split array. We also plan to design a comparator optimized for low-power operation and to provide a serial output to the ADC data.

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