Nano-Watt silicon-on-sapphire ADC using 2C-1C capacitor chain

Z. Fu, P. Weerakoon and E. Culurciello

An analogue-to-digital converter (ADC) in a 0.5 μm silicon-on-sapphire CMOS technology is reported. This innovative ADC uses a 2C-1C capacitor chain and a switched capacitor comparator. The ADC is capable of sampling at 409 kS/s, consuming 900 nW at 1.1 V power supply and 1.35 μW at 1.5 V. It uses an active area of 300×700 μm^2 and 640×1070 μm^2 with pads.

Introduction: Recent years have witnessed remarkable progress in the field of untethered sensors. Many pioneering applications have demonstrated that networks of sensors can greatly advance scientific efforts to understand indoor, natural, civil and tactical environments by providing information from locations that were not reachable before [1]. For wireless sensors, power management is one of the most crucial bottlenecks of the design. Because of the limitation of battery operation in long-term deployments of sensors, self-powered systems have become increasingly attractive [2]. Solar cells and microelectromechanical systems (MEMS) have been widely used in many self-powered systems since their fabrication methods can be combined with IC technology. Because chip-sized energy scavenging devices can provide limited power, sensory circuitry should be designed for ultra-low power budgets [3, 4]. As the interface between the sensing environment and the digital processing module, analogue-to-digital converters are crucial to the energy scavenging sensor system's performance. In this Letter we report an ultra-low power analogue-to-digital converter, which is innovative from three standpoints. First, a 2C-1C capacitor chain implementation is reported, owing to its compact silicon-area and low power consumption. Secondly, a switched capacitor with cascoded inverter is chosen as a high-speed and ultra-low power comparator. Thirdly, because of the combination of the above innovations, this ADC has a power consumption as low as 900 nW at 1.1 V power supply and 1.35 μW at 1.5 V. A recent publication [5] presented a good example of a sub-μW ADC (ADC consumes power less than 1 μW). This Letter focuses on a sub-μW ADC with much larger input range ratio over power supply. When sampling at the same speed of 150 kS/s and a 1 V power supply, this 2C-1C ADC consumes as low as 20% of the power consumed by [5].

A conventional successive approximation architecture is chosen because the simplicity of the design allows for low power consumption, while keeping the sampling rate at high speed. Fig. 1 shows the successive approximation ADC implemented with a 2C-1C capacitor chain. A linearly scaled voltage is delivered by setting and resetting the successive approximation registers. A binary search through all possible quantisation levels is performed before converging to a final digital answer, which is stored in the successive approximation registers.

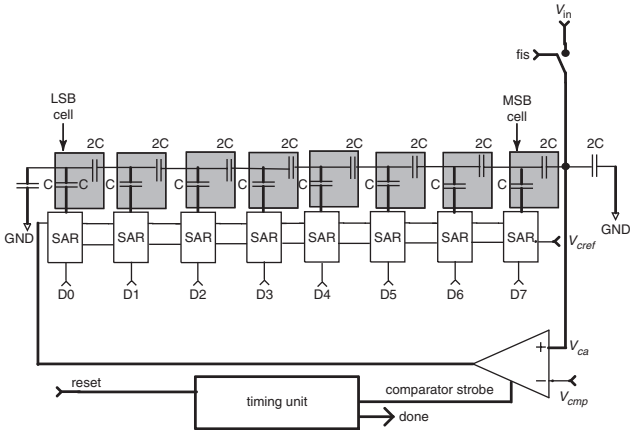

Fig. 1 *Successive approximation register (SAR) and 2C-1C capacitor chain*

2C-1C capacitor chain: As shown in Fig. 1, the capacitor chain is composed of eight identical capacitor cells and two grounded capacitors at either end. Each capacitor cell includes a floating 2C capacitor and a 1C capacitor, which is driven by the successive approximation register (C is the unit capacitance in the chain). The 2C capacitor is floating because it is not directly charged or discharged by a voltage source. In the bulk CMOS process, the floating plate couples with the substrate forming parasitic capacitance, which corrupts the ADC performance at high speed. The silicon-on-sapphire (SOS) process is immune to this problem because its substrate is an insulator. The MSB and LSB capacitor cells are connected to ground via a 2C capacitor and a 1C capacitor, respectively. The 2C-1C capacitor chain has three advantages over a conventional binary scaled capacitor array. 1. The 2C-1C capacitor chain is compact compared to a conventional full capacitor array. In an 8-bit ADC, a 2C-1C capacitor chain needs 27C, while a binary-scaled capacitor array needs 256C. 2. Because of edge effects, parasitic capacitances and manufacturing tolerances, it is difficult to make capacitance precisely scaled by the power of 2. All 2C-1C capacitor cells in the chain are identical, so a precise binary-scaling of the capacitance is not necessary. 3. Because capacitors driven by SARs are smaller, charging and discharging of the capacitors consume less power.

The output of the capacitor chain V_{ca} is the voltage between the floating 2C capacitor in the MSB cell and the grounded 2C capacitor at the same end. It is expressed in (1):

$$V_{ca} = V_{\text{in}} + \sum_{k=1}^{N} \frac{D_k 2^{N-k}}{2^N \times 3} V_{cref} \tag{1}$$

where N is the total number of bits in the ADC (eight in this case). D_k is the digital bit stored in the kth successive approximation register. The capacitor reference voltage V_{cref} is the voltage of the capacitor bottom plate when the successive approximation register is set to 1. The capacitor reference voltage V_{cref} was set to 1.6 V with a 1.1 V power supply and 2.3 V with a 1.5 V supply.

Switched capacitor comparator: To minimise the power consumption in the comparator, which is the most power hungry component in the ADC, we used a switched capacitor comparator based on a cascoded inverter [6]. A cascoded inverter implementation offers two advantages over the basic common-source amplifier: first, a higher gain owing to the larger output resistance; secondly, a higher operational speed owing to the reduced Miller capacitance. The schematic of the comparator is shown in Fig. 2. Two pMOS and two nMOS are connected in series. M_4 is separated by a capacitor from the input, which switches between the input signal V_{ca} and the reference voltage V_{cmp}. Three transistors, M_1, M_2 and M_3, operate at the subthreshold region for higher device gain. These biases are 0.6 V, V_{dd} and 0 V, respectively. Two intrinsic transistors [7] were used for M_2 and M_3 to eliminate the need of additional biases for the cascoded inverter. A correlated double sampling (CDS) technique [8] was used in the comparator to eliminate the correlated noise and the mismatch in devices. A comparison is obtained after two phases. 1. Reset phase: switches S_1 and S_2 are closed, while switch S_3 is open. The reference voltage V_{cmp} is stored on the capacitor C_s, together with any correlated noise. The inverter is also initialised to its logic threshold. 2. Compare phase: switch S_3 is closed, while switches S_1 and S_2 are open. The input V_{ca} is connected and the comparator changes its state when this voltage exceeds V_{cmp}. Simulations indicate that the comparator consumes as low as 200 nW while operating at 10 MHz.

Results: The analogue-to-digital converter was fabricated with a commercially available 0.5 μm silicon-on-sapphire process ($V_{tn} = 0.7$ V, $V_{tp} = -0.8$ V) offered by Peregrine [7]. The process features three metal layers, including a metal-thick layer for high quality passive capacitors, as well as a single polysilicon layer. The die size is 300×700 μm^2 and 640×1070 μm^2 with pads. The converter operates at 1.1 to 1.5 V power supply. The comparing reference voltage V_{cmp} was set to 1 V for 1.5 V power supply and 0.8 V for 1.1 V.

Fig. 3 shows the analogue and digital power consumption at different frequencies. The power for analogue components provides the current for charging and discharging of the capacitors and operating of the comparator. The power consumption is 900 nW at 1.1 V supply and 1.35 μW at 1.5 V supply when the converter operates at 4 kS/s. The digital power supplies the control logic and output buffers and increases

linearly with the operational frequency. At higher clock rate, more power is consumed to drive the 50 pF capacitive load of testing equipment. The digital power becomes negligible when the ADC is used in a system-on-chip.

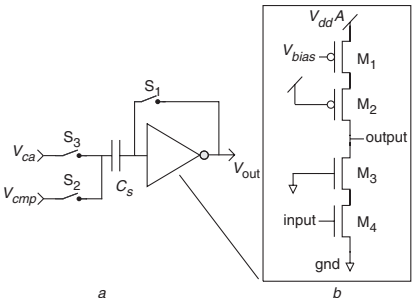

Fig. 2 *Switched capacitor comparator based on cascoded inverter and cascoded inverter implementation*

a Switched capacitor comparator based on cascoded inverter
b Cascoded inverter implementation

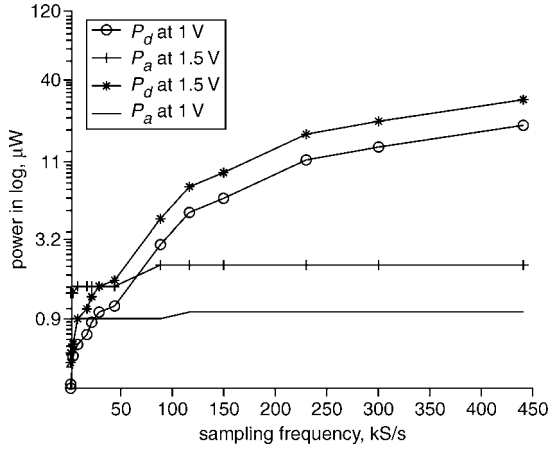

Fig. 3 *Power consumption against operational frequency at 1.1 and 1.5 V power supply*

P_a is analogue part of power consumption, P_d is digital part of power consumption

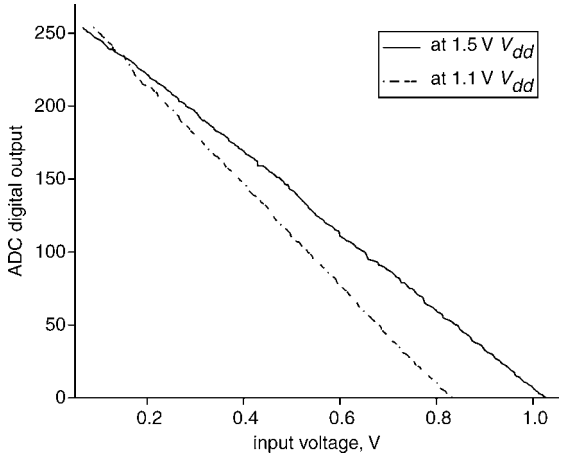

Fig. 4 *Transfer function curve between analogue input and digital output at 1.1 and 1.5 V power supply*

The analogue-to-digital converter operates from 22 kHz to 4.5 MHz clock rate, which corresponds to a sampling rate from 2 to 409 kS/s. Fig. 4 shows the transfer function curve of the ADC with a 1.1 and 1.5 V power supply. The data is collected at a clock frequency of 89 kHz corresponding to a sampling frequency of 8.9 kS/s. The input range was measured as 0.97 V for 1.5 V and 0.84 V for 1.1 V. The analogue-to-digital converter performed with an average 0.70 LSB differential nonlinearity (DNL) and an average of 1.02 LSB integral nonlinearity (INL) at 1.5 V power supply and 0.67 LSB DNL and an average of 0.9 LSB INL at 1.1 V power supply. Because of this ADCs extremely low power property, it is well suited for wireless sensors powered by energy scavenging systems and systems that require moderate precision but long duration of operations.

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