16 × 16 pixel silicon on sapphire CMOS digital pixel photosensor array

E. Culurciello and A.G. Andreou

A report on a 16 × 16 pixel digital pixel photosensor array fabricated in silicon on sapphire CMOS technology is presented. The integrated current from integrated *pin* photodiodes is converted into a pulse density modulated address event stream at the pixel level. An arbitrated asynchronous interface is employed to output the digital data. The transparency of the sapphire substrate allows imaging from both the back and front side, opening possibilities for new and novel applications of CMOS photosensor arrays.

Introduction: Silicon on sapphire (SOS-CMOS), is a flavour of silicon on insulator technologies where the transparency of the sapphire substrate to optical wavelengths from infrared to ultraviolet, opens unique opportunities for highly integrated optoelectronic microsystems [1]. Examples are integrated adaptive optical wavefront correction [2] systems for laser free space communication and an occular prosthesis device [3]. The electrically insulating properties of the sapphire substrate yields transistors with low parasitic capacitances and circuits that can be operated at high speed with low power dissipation [4].

In this Letter we report on a 16 × 16 pixel photosensor array for a microscale adaptive wavefront correction application. The chip is fabricated in the 0.5 µm process SOS-CMOS technology from a Peregrine semiconductor [5].

Sensor architecture: Digital representation of light intensity at the pixel level has been employed in the past for large dynamic range, low-power CMOS imagers [6, 7].

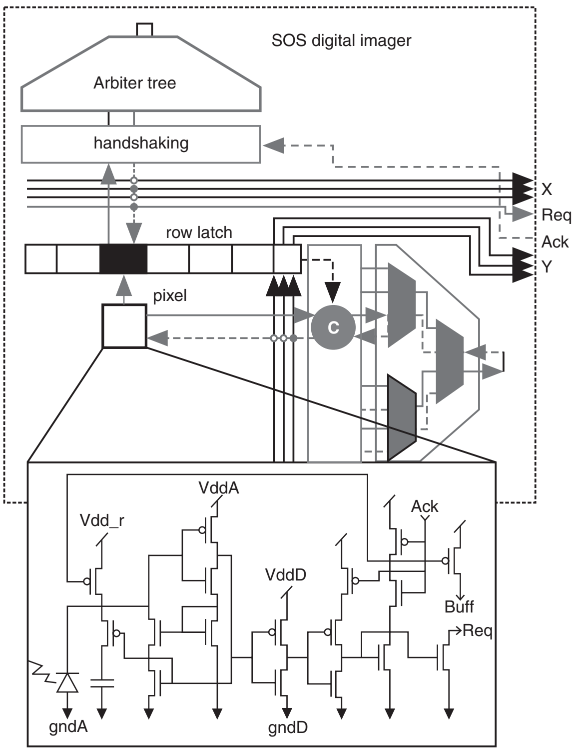

Fig. 1 *SOS-CMOS digital pixel photosensor array architecture*

The digital pixel photosensor array described in this Letter employs pulse frequency modulation at the pixel level converting the analogue data into asynchronous digital address events. Individual pixels integrate light on a local capacitor and when a threshold is reached they request access to the output bus, and their address (X, Y locations) appears at the output after arbitration (refer to Arbiter tree in Fig. 1) in the form of an event. The value of the light intensity is inversely proportional to the inter-event interval. The sensor array read-out is initiated by individual pixels, therefore the available output bandwidth is allocated according to pixel demand. A detail analysis and comparison of synchronous and asynchronous event based read-out schemes is beyond the scope of this Letter and can be found in [8].

Pixel and photodiodes: A native *pin* photodiode is employed as the pixel's photosensitive element. The spectral and temporal characteristics of these diodes have been reported in [9]. Using the ultra-thin silicon photodiodes has advantages and disadvantages. Photon absorption in the ultra-thin (100 nm) silicon layer is small, thus severely degrading the quantum efficiency with a spectral sensitivity mostly in the short wavelengths (blue and UV). This is in contrast to bulk CMOS photodetectors that are sensitive to red and infrared and have weak response to blue. In the intended application where the sensor array is not employed for imaging but rather in the feedback loop of a wavefront correction system, this is not a problem. Using a *pin* photodiode in conjunction with the insulating substrate decreases the photodiode capacitance yielding devices with bandwidth in excess of 5 GHz [9]. The photodiode used in our pixel has a horizontal structure 100 nm thick and 16.4 µm long, with a 1.2 µm intrinsic silicon layer between anode and cathode. The photocurrent is integrated on a 250 fF capacitor.

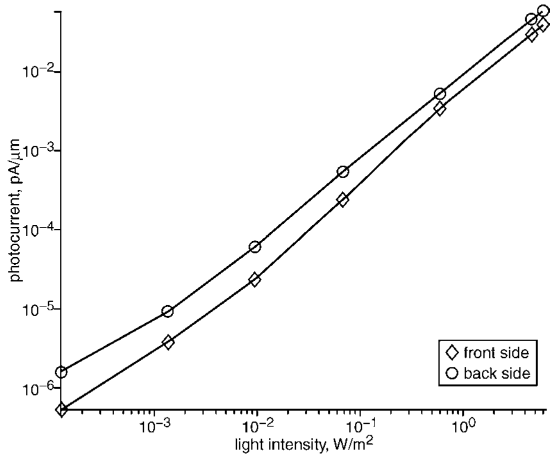

Fig. 2 *Front and back side photocurrent at 555 nm*

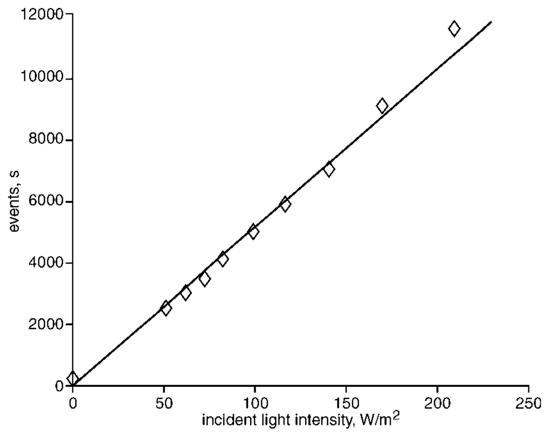

Fig. 3 *Event rate against light intensity*

Fig. 2 shows a plot of the photocurrent per unit length of the SOS *pin* photodiode from both front and back side of the die. Light intensity was measured with a photometer and a variable high intensity source at 555 nm. Note that light integrated from the back side generates higher photocurrents than the front side. This occurs because the front side of the die is covered by metal and SiO_2 layers that filter some of the incident light. Fig. 3 shows the spike frequency against incident light intensity for a single pixel in the array. Using backside illumination achieves 100% fill factor. For the data in this Figure, the light was focused on a single pixel on the array using a lens, and the light intensity was varied using neutral density filters. The event frequency

f_{ev} is linear with light intensity I_{in}. The relationship is given in (1) where the parameter L_s equals to 51:

$$f_{ev}\ [\mathrm{Hz}] = L_s \cdot I_{in}\left[\mathrm{W/m^2}\right] \quad (1)$$

The output event frequency spans approximately two orders of magnitude (200 to 11 500 Hz) and thus the array is capable of encoding data with 4 to 6 bits of precision, which is more than adequate for the intended application.

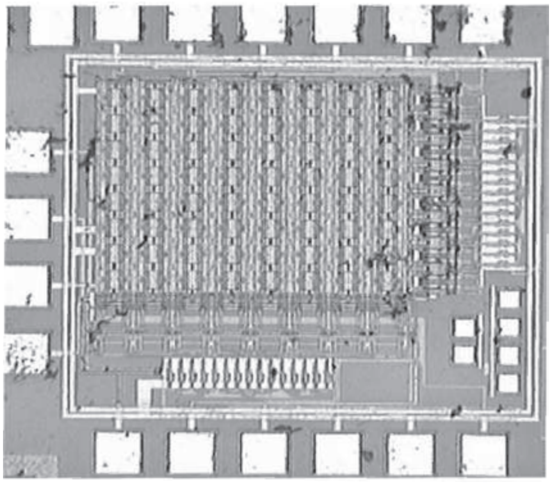

Fig. 4 *Die micrograph for 16 × 16 sensor array*

The die area for the sensor array is 0.66 cm^2 without output pads, and 1.23 cm^2 with pads. Pixel size is 29.6 × 42 µm. A micrograph of the die is shown in Fig. 4. The SOS wafer was polished only on the front side after fabrication. To obtain a clear die on both sides, the back side of the die has been polished using a mechanical lapping machine. Lapping was performed up to a surface roughness of 1 µm. The mechanical polishing resulted in an optically clear die. Alternatively index matching fluid can be employed to fill in the asperities of the backside surface [1].

Acknowledgments: Fabrication was provided by MOSIS through a DARPA fabrication grant, R. Athale was our point of contact. This work was supported by NSF grant Microscale Adaptive Optical Wavefront Correction, ECS-0010026.

 14 October 2003

Electronics Letters online no: 20040055
doi: 10.1049/el:20040055

E. Culurciello and A.G. Andreou (*Department of Electrical and Computer Engineering, Johns Hopkins University, Baltimore, MD 21218, USA*)

References

1 Andreou, A.G., *et al.*: 'Silicon on sapphire CMOS for optoelectronic microsystems', *IEEE Circuits Syst. Mag.*, 2001, **1**, (3), pp. 22–30
2 Cohen, M., *et al.*: 'Adopt: analog VLSI stochastic optimization for adaptive optics'. Proc. Int. Joint Conf. Neural Networks (IJCNN'99), Washington DC, USA, 1999, Vol. 4, pp. 2343–2346
3 Uehara, A., *et al.*: 'Back-illuminated pulse-frequency modulated photosensor using silicon-on-sapphire technology developed for use as epi-retinal prosthesis device', *Electron. Lett.*, 2003, **15**, pp. 1102–1104
4 Andreou, A.G., and Abshire, P.: 'Sensory communication microsystems: analysis and synthesis framework'. Tech. Rep. JHU-ECE-01/01, Department of Electronic and Computer Engineering, Johns Hopkins University, Baltimore, MD, 2001
5 Peregrine Semiconductors Inc.: '0.5 µm FC design manual (52/0005)', March 2003 (URL: http://www.peregrine-semi.com/)
6 Boahen, K.A., Culurciello, E., and Etienne-Cummings, R.: 'A biomorphic digital image sensor', *IEEE J. Solid-State Circuits*, 2003, **38**, (2), pp. 281–294
7 Kleinfelder, S., *et al.*: 'A 10 000 frames/s CMOS digital pixel sensor', *IEEE J. Solid-State Circuits*, 2001, **36**, (12), pp. 2049–2059
8 Culurciello, E., and Andreou, A.G.: 'A comparative study of access topologies for chip-level address-event communication channels', *IEEE Trans. Neural Netw.*, September 2003 (Special Issue on Hardware Implementations)
9 Apsel, A., *et al.*: 'Thin film *pin* photodiodes for optoelectronic silicon on sapphire CMOS'. Proc. 2003 Int. Symp. on Circuits and Systems, ISCAS'03, May 2003, Vol. 4, pp. 908–911