A Four-Channel Integrated Patch-Clamp Amplifier with Current-Clamp Capability

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***Abstract*—We present the first fully-integrated microchip implementation of a patch-clamp measurement system featuring both current clamp and voltage clamp modes with gain control, leak correction, series access resistance compensation, parasitic capacitive compensation capability, and input and output filters. The system was implemented in a 1-poly, 3-metal, 0.5 μm Silicon-on-Sapphire process. In voltage clamp mode input-referred rms noise was measured at 3.3 pA in a 5 kHz bandwidth and in current clamp mode input-referred rms noise was measured at 150 μV in the same bandwidth. The system can compensate for the capacitance and resistance of the electrode, up to 10 pF and up to 80% of the series access resistance of 100 MΩ respectively, or 100% with phase-lag compensation. Four fully integrated dual clamp channels are contained on one 4 mm by 8 mm die. The power consumption is 30.1 mW per channel at 3.3 V.**

I. Introduction

Electrophysiologists commonly use the current clamp and voltage patch-clamp techniques for the study of ion channels, which are the molecular structures responsible for membrane conductivity [1] [2]. In a planar electrode array, tens or hundreds of whole cell patch clamp recordings can be performed, requiring small integrated amplifiers [3]. In a current clamp experiment, a known current is applied, often mimicking the current produced by synaptic input, and the resulting changes in the membrane potential are measured. This is a useful technique for measuring the voltage response of a cell, such as action-potentials [4]. In a voltage clamp experiment, a known voltage is applied to the membrane and the resulting transmembrane current is measured. While this does not mimic a process found in nature, if the transmembrane voltage determines channel gating, then it offers control of the opening and closing of ion channels, and allows one to resolve currents flowing through ion channels [5]. The currents measured by the patch-clamp are used to study the effect of medical compounds and the behavior of ion channels, the structures responsible for cell membrane conductivity [6].

Since the currents are so small, the electronic amplifier used to measure the currents must be carefully designed to avoid adding appreciable noise to the measurement. It is also important that the amplifier be capable of compensating for the measurement error introduced by the electrodes.

While bench-top systems exists for this purpose by manufacturers such as [7], [8], and [9], they are bulky and expensive and not well suitable for multichannel high-throughput systems. We present a single integrated circuit that is capable of both voltage-clamp and current-clamp and can be used to fabricate multi-channel high-throughput systems. A single integrated circuit is desirable because it is smaller and more suitable for use with a planar electrode array, it reduces noise and power consumption, and offers better electrical performance.

Although integrated circuits able to measure whole-cell currents have been previously realized, they lack the essential ability to compensate for the resistance and the parasitic capacitance of the electrode [3], [10], and [11]. We previously presented an integrated system that added this capability, [12], but did not include current clamp functionality. This work adds current clamp capability and is the first system to offer leak compensation in current clamp mode. Additionally, it brings 4 channels to the chip, making it more desirable for use in a high-throughput system, and has a decreased overall system noise compared to our previous design, allowing for more accurate recording.

II. Patch-Clamp System Overview

Each channel of the patch clamp amplifier can be set by the user via digital configuration in either voltage or current clamp mode, which controls switches to reconfigure the circuit for either operation as shown in Fig. 1. As shown the switches are configured for the circuit to be used in voltage clamp operation, and toggling them will result in current clamp operation.

In voltage clamp mode, the headstage of the patch-clamp recording system consists of a current-to-voltage transimpedance amplifier (TIA) that uses resistive feedback with a user-selectable R_f. A difference amplifer (Diff Amp) subtracts V_{clamp} from the transimpedance output. The resultant output voltage is proportional to the input current.

In current clamp mode, the TIA is configured as a unity gain buffer, the opamp in the Diff Amp is configured as a voltage subtractor, and the R_S compensation circuits are disconnected. The injected current is then V_{clamp}/R_f and can be supplied to the chip in the same fashion as the stimulus in the voltage clamp mode. The resultant output voltage is a buffered form of the input voltage. Note that leak compensation can still be applied in this mode.

The electrode compensation circuitry used in this system has previously been presented in [12].

The system makes use of a high-performance, low-noise, rail-to-rail, constant-transconductance operational amplifier design, as previously presented in [13]. The amplifier was

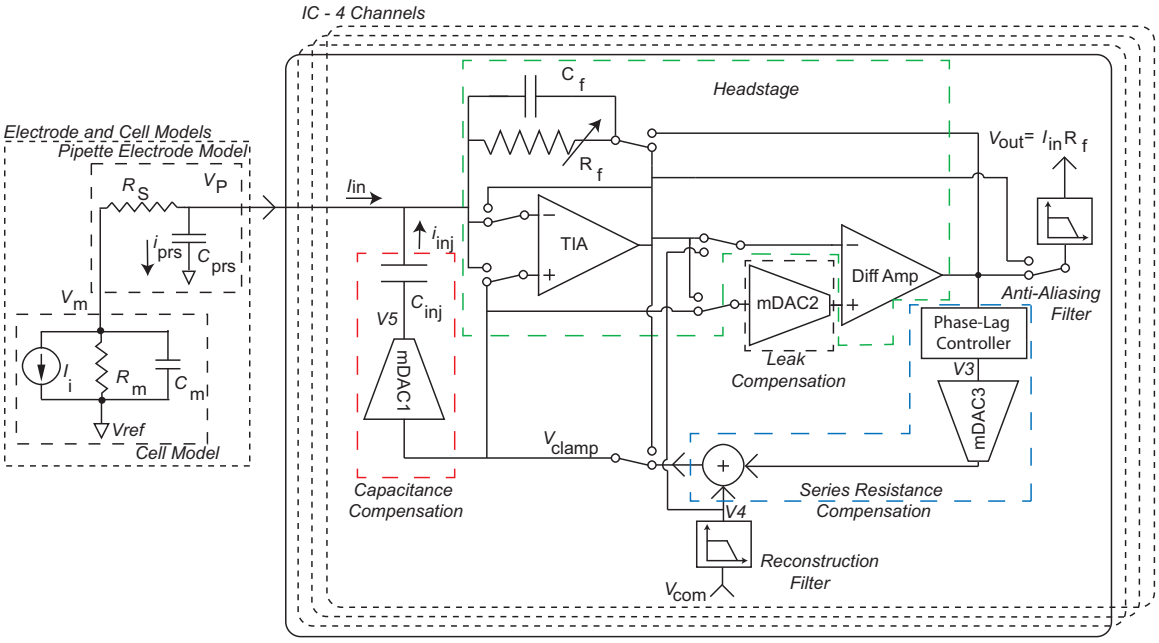

Fig. 1. Dual clamp reconfigurable integrated circuit circuit, switch positions for the channel shown are configured in voltage clamp mode, the other switch setting is for current clamp. R_f is selectable and has 12 values ranging from 49 kΩ to 100 MΩ. Leakage current subtraction is provided by using mDAC2 to vary the common mode of the Diff Amp. Compensation for the capacitance and resistance of the electrode is provided by mDAC1 and mDAC3 to compensate for up to 10 pF and up to 80% of the series access resistance of 100 MΩ.

updated for this design to have lower noise by increasing transistor sizes. Constant transconductance is required in order to perform linear compensation protocols over the entire rail-to-rail, common mode range. Rail-to-rail operation of the amplifier is required for a high V_{clamp} with high R_S compensation and for improving the system's the signal-to-noise ratio.

The designed amplifier was fabricated in a 0.5 μm SOS process and the die micrograph is shown in Fig. 2 with each functional block labeled.

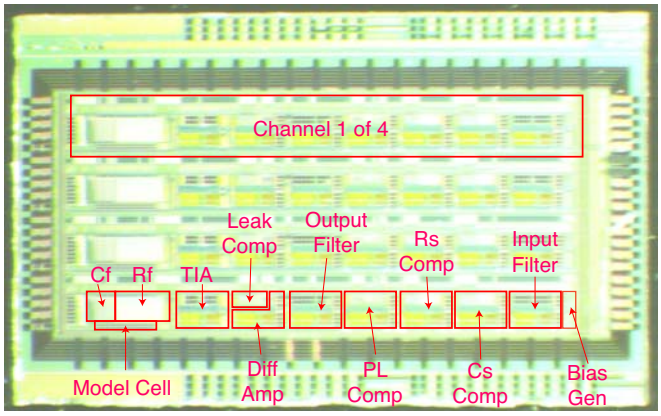

Fig. 2. Micrograph of the manufactured 4 channel integrated voltage and current patch-clamp amplifier die, dimensions 4mm by 8mm.

III. Hardware Test-Bed

The hardware test-bed consists of two stacked circuit boards and was packaged in a grounded shielded box to reduce the impact of external environmental noise. The entire system is powered at 3.3 V using a USB bus and the digital interface was provided using a Xilinx Spartan-3 field programmable gate array (FPGA) on an Opal Kelly XEM3001 board. The command voltage was provided by an Analog Devices 16 bit AD5668 digital to analog converter (DAC). The output of the amplifier was digitized using a 16 bit Analog Devices AD7685 analog to digital converter (ADC). The patch-clamp chip and these peripherals are installed on a custom designed 4-layer printed circuit board (PCB) which interfaces to the Opal Kelly board. The data was sampled at 100 kHz after the on chip 20 kHz 2-pole low-pass filter. A GUI driven C++ program running on a laptop computer allows configuration of the chip in either voltage clamp or current clamp mode, the compensation mDACs to be set, stimulus pulses to be generated, and the output signals to be acquired and plotted.

IV. Measurement Results

The performance of the system was measured in both voltage clamp and current clamp mode. In voltage clamp mode, the whole channel's input-referred RMS current noise was measured with a 100 MΩ feedback resistor by floating the input and tying the command voltage to the experimental ground, V_{ref}, and was 3.3 pA in a 5 kHz bandwidth, and its power spectral density is shown in Fig. 3. The input capacitance was measured at 3.96 pF, and the leakage current was measured at 23 pA. The input capacitance was measured by applying C_s compensation while observing the output until the capacitance was compensated and noting the value. This measurement includes the input of the amplifier, the bonding pad, and the trace on the PCB to the input pin. The leakage

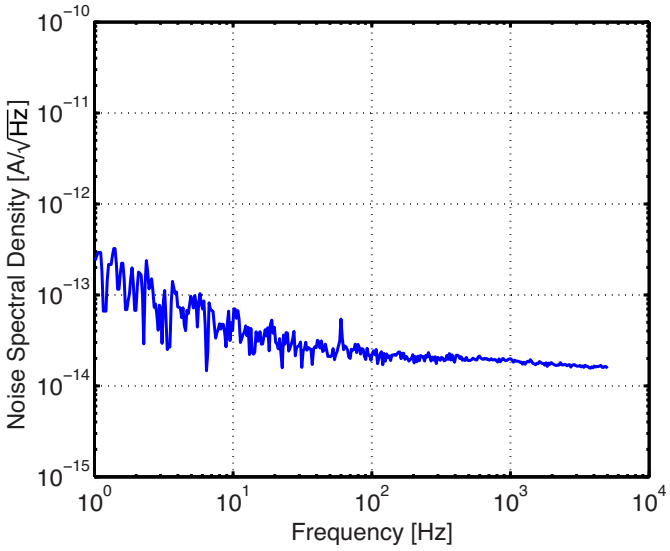

Fig. 3. Measured input-referred current noise spectral density of the amplifier in voltage clamp mode with an input capacitance of about 4 pA and 23 pA of leakage current.

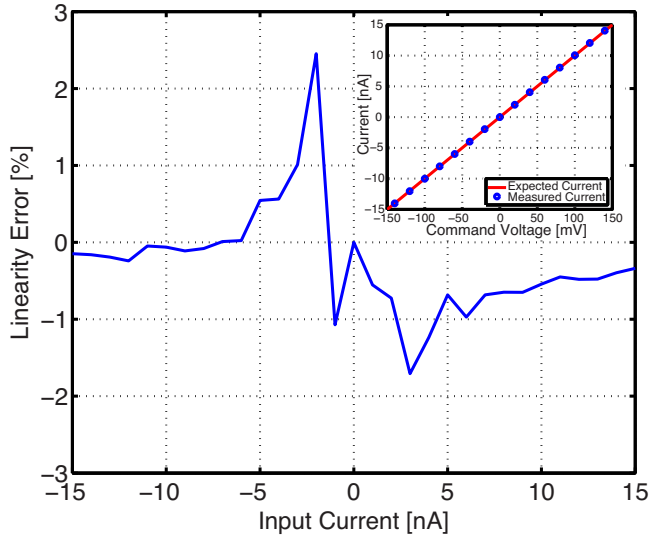

Fig. 4. Measured linearity error as a percentage of the input current in voltage clamp mode. The data was taken when R_f was 100 MΩ by sweeping the command voltage and measuring the input current across a 10 MΩ resistor and comparing it to the expected current.

was measured by floating the input pin, setting V_{clamp} to V_{ref}, and converting the output voltage to input current by dividing by R_f. The linearity of the measurement in voltage clamp mode was determined by sweeping the stimulus V_{clamp} when a known test resistor was placed between the input and V_{ref} while measuring the output and converting it to input-referred current by dividing the average value of 1000 samples by R_f for each point. After zeroing and applying a constant correction factor to compensate for the test resistor and the feedback resistor deviating from their nominal values, the system shows excellent linearity as shown in Fig. 4.

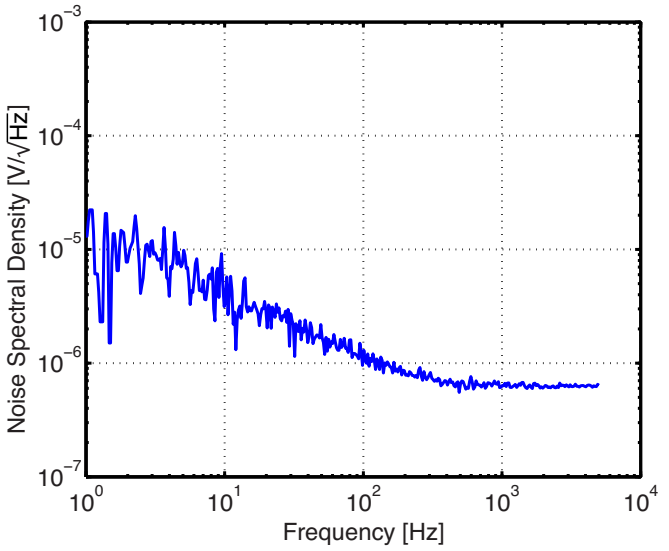

Fig. 5. Measured input-referred voltage noise spectral density of the amplifier in current clamp mode with an input capacitance of about 4 pA and 23 pA of leakage current with a 10 MΩ input resistor.

In current clamp mode, the input-referred RMS voltage noise was measured with a 100 MΩ feedback resistor and a 10 MΩ input resistor and was 150 μV in a 5 kHz bandwidth and its power spectral density is shown in Fig. 5. The linearity of the measurement in current clamp mode was taken similarly to the voltage clamp case, by sweeping the input current and measuring the output voltage. Again, the system shows excellent linearity as shown in Fig. 6.

To test the new current clamp with leak compensation functionality, a model cell consisting of a 1 GΩ resistor in parallel with a 22 pF capacitor was used with a 10 MΩ series resistance, along with an optional leakage resistance of 100 MΩ and is shown in the top left of Fig. 7. The feedback resistor was chosen as 12.5 MΩ and two experiments were performed. In each experiment, after 10 ms, a 10 mV pulse was applied to generate 800 pA of clamping current and the voltage was recorded. The first experiment was performed with the leakage resistor without leakage compensation, and in the second experiment the leakage compensation was enabled. The stimulus is shown in the top right and the measured voltage across the model cell during each experiment is shown in the bottom of Fig. 7 which shows that the system can compensate for leakage current. This device reports similar performance to bench-top devices as the Axopatch 200B in whole cell configuration.

Cross-talk measurements were taken by applying a ±30 mV voltage stimulus across a 10 MΩ resistor to one channel and observing the measured current on neighboring channels, and results with a 100 MΩ feedback resistor are shown in Fig. 8, which indicates cross-talk is not an issue.

V. Conclusion

The testing results of the addition of current clamp mode to our previously reported patch-clamp amplifier indicate that

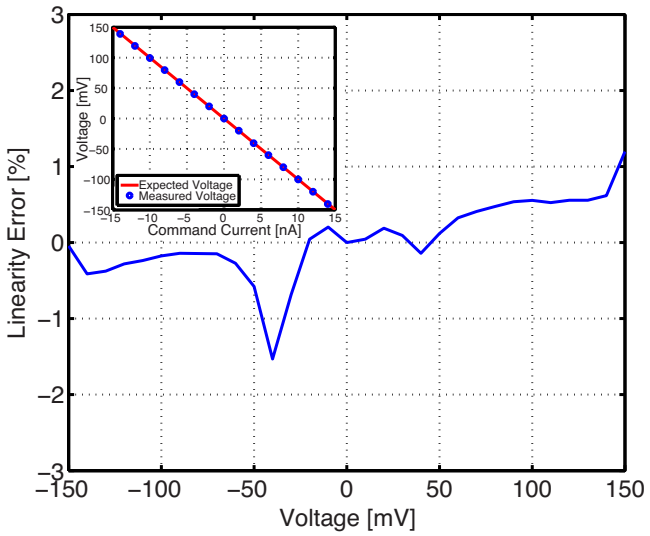

Fig. 6. Measured linearity error as a percentage of the output voltage in current clamp mode. The data was taken when R_f was 100 MΩ by sweeping the command current and measuring the output voltage across a 10 MΩ resistor and comparing it to the expected voltage.

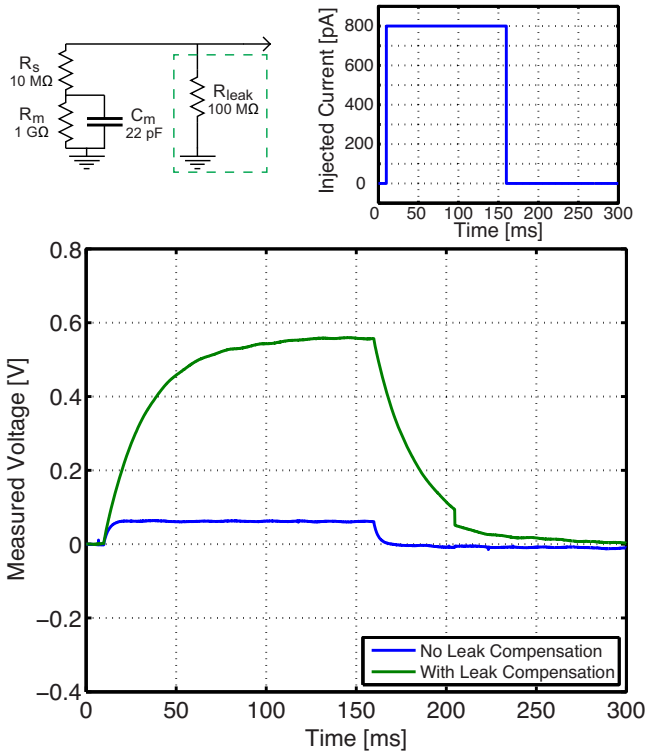

Fig. 7. Measurements in current clamp mode with leak compensation on electrical model cell, model cell shown in top left, applied stimulus shown in top right. The experiment was performed with the leakage resistor without leakage compensation and then the compensation was enabled.

this is an excellent solution as it performs similar to bench-top devices during whole cell recording and provides similar features and performance at reduced size, cost and power consumption, and is ready for use in fabricating a high-throughput planar patch-clamp system.

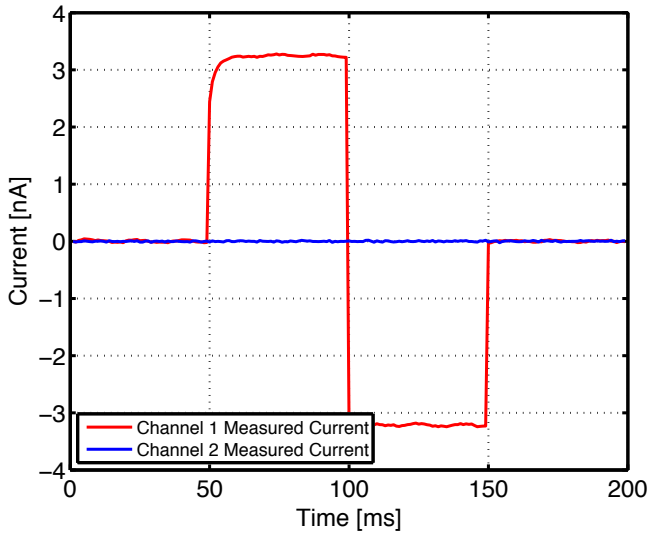

Fig. 8. Measured Crosstalk between Channels 1 and 2 when channel 1 experienced a stimulus while channel 2 did not.

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