A 1-mW CMOS Temporal-Difference AER Sensor for Wireless Sensor Networks

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***Abstract*—In this paper, we report a 64 × 64 active pixel sensor, designed for low-power image sensing for wireless sensor networks. The proposed image sensor computes the temporal difference between two continuous frames and communicates them in an address–event representation format. The image sensor is capable of computing 30 temporal-difference frames per second (fps) and consumes 1 mW with a 3-V power supply. Light-intensity images are also available as an output at a speed of 60 fps. The image sensor was fabricated in a 0.5-μm bulk CMOS process. The fabricated sensor was tested with various stimuli to evaluate its performance. The die size is 3 mm × 3 mm, including pads and test structures. Each pixel occupies an area of 29 × 28 μm^2 with a fill factor of 23%. The minimum detectable speed of the temporal-difference is 4.5°/s.**

***Index Terms*—CMOS image sensor, low power, smart image sensor, smart sensor, temporal difference, wireless sensor networks (WSN).**

I. Introduction

WIRELESS sensor networks (WSNs) have a significant impact on advanced sensing technologies and a wide range of applications ranging from military, to scientific, industrial, health care, and home. Ubiquitous WSN will pervade society and redefine the way in which we live and work [1]–[4]. A group of wirelessly connected sensing devices can collaborate and collect raw local data, producing globally meaningful information. Within all sensing devices, an image-sensor system usually provides us with a large amount of information that the others cannot. At the same time, the emergence of new generations of radios, smaller and more energy efficient microcontrollers, and constantly expanding networking support are enabling people to consider the deployment of sensor networks in everyday-life applications such as assisted living (fall detection) [5], workplace safety, and entertainment. On the other hand, the use of image sensors in sensor networks is restricted by their resource bottleneck. Image sensors are power hungry and require significant resources in computation, storage, and communication bandwidth. A commercial off-the-shelf (COTS) imager usually requires tens of milliwatts to capture snapshots. It demands much more power in computation, storage, and communication resources to further process and communicate these images to outside receivers.

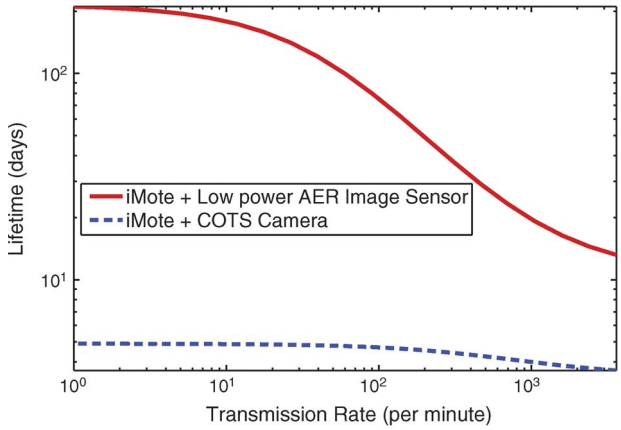

Fig. 1. Lifetime comparison between an iMote node using a customized image sensor and that using a COTS low-power image sensor. The proposed customized image sensor has an on-chip signal-processing capability and increases the sensor-node's lifetime by an order of 100 times [13].

Over the last decade, research on CMOS image sensors has focused on increasing the imager resolution and its speed [6], [7], whereas there has been little research to reduce the power consumption [8]. A high-quality image delivers high-fidelity visual information, but the information requires additional resources to compute, transmit, and store them. In particular, when a video is streamed through a bandwidth-limited wireless channel to understand the content of a scene, the abundant data of the high-resolution images become cumbersome and inefficient to handle [2]. Although downsampling techniques can usually be employed to reduce the bandwidth requirements, they require additional computation time, power, and resources. Recent studies have indicated that a custom image sensor can integrate circuits for basic decision making and image compression with low power [9], [10] and can increase a sensor-node's lifetime by two orders of magnitude [11]. Fig. 1 shows the lifetime comparison between an iMote2 sensor node [12] using the proposed custom image sensor and another iMote2 sensor using a COTS low-power image sensor (Omnivision OV7649). The proposed image sensor has two different properties from a COTS imager: First, it consumes 1 mW of power or less in active state. Second, it is able to compute the temporal difference between continuous frames and filter out redundant data. In fact, an iMote2 node consumes 400 times more power in active state than in sleep mode. The microprocessor unit and the radio-communication components on a sensor node stay in a sleep state when the proposed image sensor captures the

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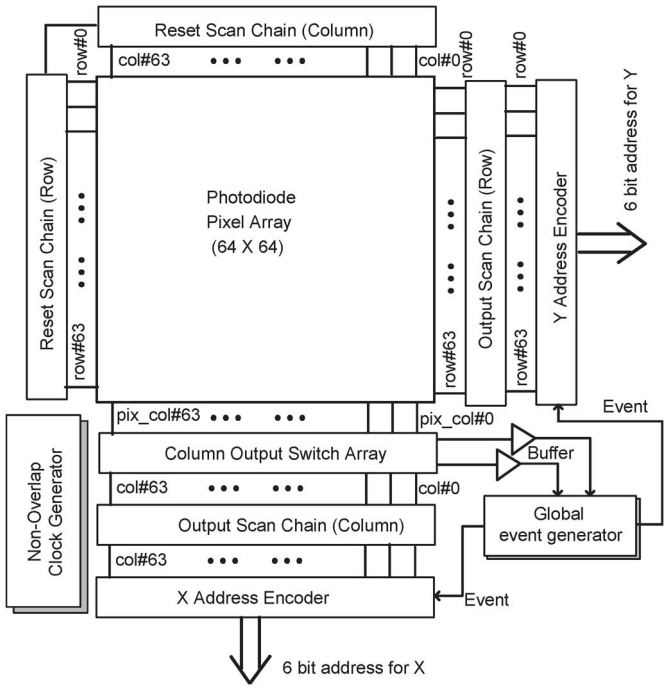

Fig. 2. Image-sensor architecture block diagram.

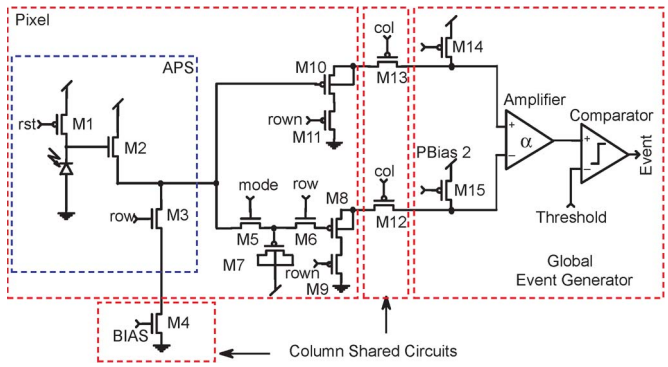

Fig. 3. Signal path from a pixel to the global temporal comparator. The APS is based on a three-transistor pixel structure. Column shared circuits are located in each column, and one global event generator is needed for the sensor.

same visual information. This low-power state continues until an exceptional event is detected, such as a light-intensity change in a significant number of pixels.

In this paper, we report a custom low-power image sensor which computes temporal difference between two continuous frames and communicates them in address–event format. The light-intensity images are also available at the same time for detailed information. This paper is divided into seven sections. In Section II, the image-sensor architecture is presented. Section III describes a signal path of the analog signal from a photodiode to the global event generator. We discuss the design concerns in the pixel's sample/hold circuit, the event-comparator design, and the event address encoder in Section IV. The experimental results are reported in Section V. The power analysis and the discussion for WSNs are presented in Section VI. Section VII concludes this paper.

II. Image-Sensor Architecture

Temporal-difference images can be obtained with a COTS camera and the digital-signal processing using an FPGA or microprocessor. However, the frame rate is limited by the analog-to-digital conversion (ADC) time and digital-signal processing. Moreover, the power consumption of an always-on microprocessor and frame memories are big burdens for wireless sensor nodes. The proposed sensor instead outputs temporal-difference frames as output. In the sensor, two continuous image frames are subtracted, and the difference is compared with two predefined thresholds to generate a temporal-difference image in an address–event format. Asynchronous address–event representation (AER) sensor [3] collects events for a fixed time to show the motion of an object, whereas the proposed sensor shows the motion information synchronously for every frame once the threshold is triggered. Fig. 2 shows the block diagram of the image-sensor architecture. The core pixel array consists of 64 $\times$ 64 photodiode pixels. The pixel array is driven by two sets of shift registers: One resets the pixels, and it is referred to as the *reset scan chain*; the other accesses the pixels and outputs their integrated signals in the photodiodes, and it is referred to as the *output scan chain*. The pixels in the array are accessed in a row-wise fashion, and the pixels in the same row are read out sequentially. When a pixel is selected by the output scan chain, the pixel outputs two analog signals through two column lines: the integrated signal of the current frame and that of the previous frame, which has been stored in the pixel. A global event generator is located outside the pixel array and generates events by the temporal difference between the two pixel values. An event is transmitted when the difference is higher than the predefined thresholds. Two address encoders at the boundary of the pixel array generate 12-b addresses of the event-generating pixel. Two amplifiers reside at the output of the array and buffer the analog signals. The clock generator provides proper nonoverlapping timing sequences to drive the scan chains and the event generator. The image sensor simultaneously outputs one digital signal and two analog signals: The digital signal reports events when the light-intensity difference in the pixels passes the thresholds; the analog signals report the selected pixel voltages for the light-intensity images. The temporal-difference image from the digital signal is represented in an address–event format.

III. Pixel Signal Path

Fig. 3 shows the signal path from the photodiode to the global event generator. The proposed pixel cell is composed of a well-substrate junction photodiode, a reset transistor (M1), a source follower (M2), selection transistor (M3), a MOS storage capacitor (M7), two switch transistors (M5 and M6), and four pMOS transistors (M8 to M11) of the column-shared pMOS followers. A pMOS transistor (M1) is used in the reset path of the photodiode because it increases the amplitude of the pixel reset voltage to $V_{\rm dd}$ and extends the pixel dynamic range. This also eliminates image lags, which is caused by incomplete resets and is evident when an nMOS reset transistor is used. However, the increased output swing comes at the expense of a larger pixel area due to the process design rule of the pMOS well. In the followers, the access transistors (M3, M9, and M11) are used to control the row sequence to access the

pixels. The access transistor (M4) is shared by the column of the pixels and controls the output sequence of the column. The global transistors (M14 and M15) are the bias transistors which act as the current sources of the source followers. Although the structure of the two column lines decreases the readout time to drive the signal into the column line with a large capacitance, the pixel area can be optimized by removing the source follower M11 and transferring the signal through the source follower M9.

The sample/hold circuit in the pixel includes two switch transistors (M5 and M6) and one hold capacitor (M7). The purpose of this circuit is to hold the pixel voltage of one frame. The capacitor is implemented with a pMOS transistor by connecting the source, drain, and bulk to $V_{\rm dd}$. A pMOS capacitor is chosen because it provides larger sheet capacitance than a metal–insulator–metal or poly–insulator–poly capacitors available in the bulk CMOS process. The switch-induced error voltage in the sample/hold circuit is caused by two factors: first, the charge injection into the hold capacitor when the switches (M5 and M6) turn off and second, the clock feedthrough due to the gate–drain capacitance in the switch transistors. In order to reduce the switching effect, the switch transistors turn off in the following order : M5, then M6, and then, M3.

Two column-shared pMOS followers are used to drive the global amplifier and compensate the dc level shift of the nMOS source follower. The source and bulk of transistors M8 and M10 are connected in order to reduce the body effect. However, this connection causes a charge coupling between the gate and bulk of transistor M8 when the output of the pMOS follower changes. This can corrupt the stored voltage on the capacitor (M7) when the pMOS follower outputs the other pixel voltages and changes its value. Since the source and bulk are connected together and the voltage of the connected node is changed when the pixel in a different row is selected and read out, the stored signal in the capacitor can be changed by the coupling of the parasitic capacitor of M8. A row-select switch transistor (M6) is employed in order to reduce the coupling effect. A global temporal comparator is located outside the pixel array to compute the temporal differences. The global event generator will be described in Section IV.

Fig. 4 shows the timing diagram when acquiring a temporal-difference image. The pixel starts the integration of the first frame after resetting the photodiode capacitor. During exposure to light, the photodiode accumulates charges depending on the incident-light intensity. After exposure, the pixel is addressed by the output scan chain. The integrated signal is stored on the storage capacitor by asserting the signal of *mode*. After a second reset, the pixel starts the integration of the second frame. The pixel outputs the second-frame integration voltage and the stored first-frame voltage when the pixel is selected again. A global event generator subtracts the two voltages and compares the difference with the thresholds.

IV. Temporal-Difference Event Generator

The temporal-difference event generator finds the difference between the pixel values in two continuous frames and outputs the events when the frame difference exceeds a threshold. As

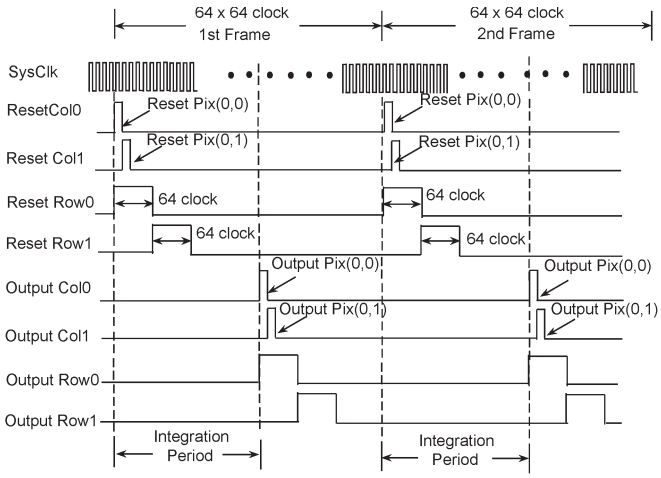

Fig. 4. Timing diagram of the proposed sensor.

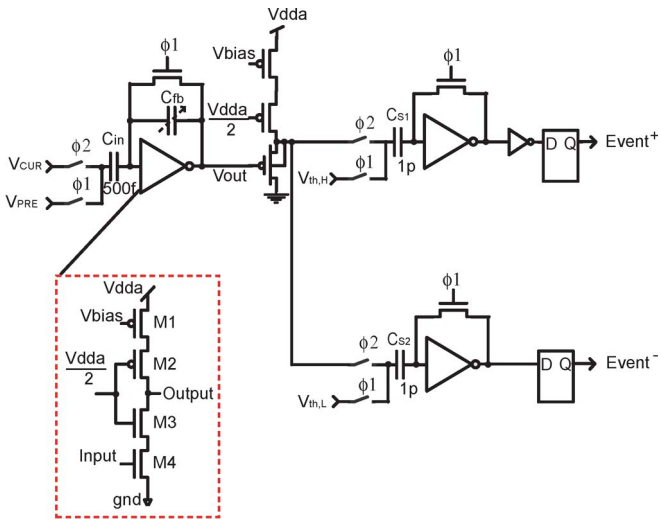

Fig. 5. Global event generator.

the proposed sensor uses the absolute temporal difference to trigger events, a small difference in dark regions should be amplified to increase the difference and generate the event. In Fig. 5, the temporal-difference event generator contains three stages: 1) an ac signal amplifier; 2) an interstage pMOS source follower; and 3) two parallel comparators. The ac amplifier in the first stage is a switched-capacitor circuit based on a cascoded inverter [14]. The cascoded inverter includes two pMOS (M1 and M2) and two nMOS (M3 and M4) connected in series. The input transistor of the inverter (M4) is separated by a capacitor with the input, which switches between the two inputs, $V_{\rm pre}$ and $V_{\rm cur}$. The biases are $V_{\rm dda}/2$ for the two middle transistors (M2 and M3) and $V_{\rm bias}$ for the top transistor (M1). The cascoded topology is used in the amplifier because it delivers two main advantages over a common-source amplifier: First, the cascoded inverter shields the input transistor from the output load, and second, the cascoded structure delivers a bigger output impedance and a larger gain. A correlated double-sampling technique was used in the circuit to eliminate the correlated noise, such as the mismatch in the devices. The ac amplifier has a variable close-loop gain of up to ten, which is set by $c_{\rm in}/c_{\rm fb}$. A pMOS follower is implemented as the second

stage to drive the two input capacitors (C_{S1} and C_{S2}) of the next stage. It also shifts up the dc level from the first-stage amplifier by the MOS threshold voltage, $V_{\rm th}$ and fits it to the comparator's input range.

An event is generated in two phases.

1) $\phi 1$ phase : Since the input voltage, V_i of the cascode inverter in the amplifier is $V_i = V_{\rm off}$, where $V_{\rm off}$ is the logic threshold of the cascode inverter, the three capacitors store the following voltages:

$$V_{\rm cin} = (V_{\rm pre} - V_{\rm off}) \tag{1}$$

$$V_{S1} = (V_{{\rm th},H} - V_{\rm off}) \tag{2}$$

$$V_{S2} = (V_{{\rm th},L} - V_{\rm off}). \tag{3}$$

2) $\phi 2$ phase : The pixel signal of the current frame is applied to the input capacitor of the amplifier, and the amplification and the comparison are performed. Since the V_i node is the virtual ground by the capacitive feedback [15], the voltage of the amplifier is decided as follows:

$$V_{\rm out} = \left(\frac{\alpha}{1 + \frac{c_{\rm in}}{c_{\rm fb}} \cdot \alpha}\right) \cdot (V_{\rm cur} - V_{\rm pre}) \approx \frac{C_{\rm in}}{C_{\rm fb}} \cdot (V_{\rm cur} - V_{\rm pre}) \tag{4}$$

where α is the gain of the inverter.

In the comparator stage, the voltage of the amplifier is shifted up by the pMOS threshold voltage and compared with two threshold voltages, $V_{{\rm th},H}$ and $V_{{\rm th},L}$. The positive and negative events are generated when $(c_{\rm in}/c_{\rm fb}) \cdot (V_{\rm cur} - V_{\rm pre}) + V_{\rm thp} > V_{{\rm th},H}$ and $(c_{\rm in}/c_{\rm fb}) \cdot (V_{\rm cur} - V_{\rm pre}) + V_{\rm thp} < V_{{\rm th},L}$, respectively.

A digital register is placed after the comparator output in order to store the comparison results and to drive the following address encoder. The proposed sensor, utilizing an event-based digital representation, outputs temporal-difference visual information [16]. AER is an asynchronous communication protocol. The proposed vision sensor transmits events when changes in pixels exceed a threshold. In the proposed sensor, a collision-detection circuit is unnecessary because pixels are polled sequentially, and only one pixel is addressed at a time. Fig. 6 shows the system of the event–address generation in the image sensor. The event signal generated by the event generator sets the *AND*-gates in the address encoder when the encoder outputs the selected pixel's address. Fig. 7 shows the schematic diagram of the simple 2-b address encoder for the column. The same 6-b address encoders are located in the row and the column, respectively. The address encoder is useful when the proposed sensor is used in the sensor-network application that needs an assignment of field of view (FOV) and the events only in the FOV are transmitted through the wireless channel.

The static logic was used in the event encoder for the low-power purpose. When an event is triggered, the selected column bits pull the transistors' drain up or down, depending on whether the address bit is "1" or "0." A minimum-sized inverter driver is used in the column inputs in order to speed up transitions of the bit states and save power.

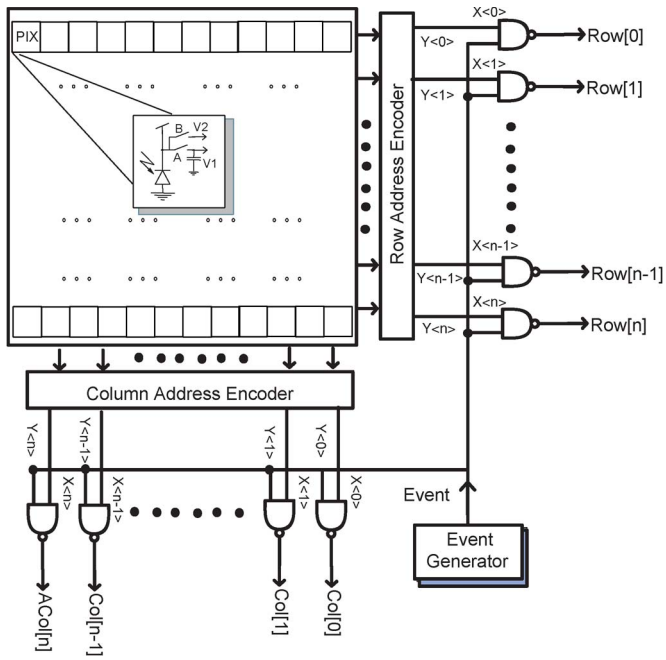

Fig. 6. Event generation in the sensor.

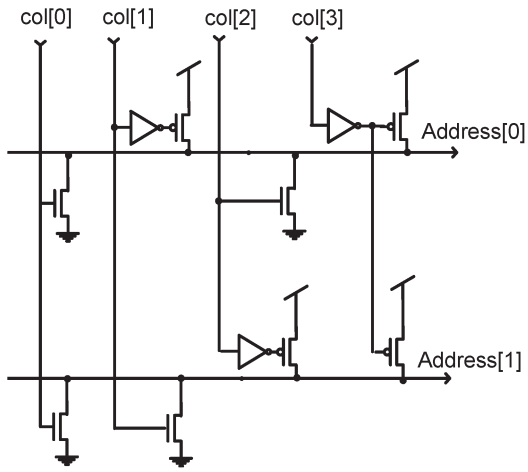

Fig. 7. Schematic of a 2-b address encoder.

V. System Experimental Performance

The sensor was fabricated in a 0.5-μm bulk CMOS process ($V_{\rm tn} = 0.75$ V and $V_{\rm tp} = -0.85$ V). The process features three metal layers and two poly layers. The die size is 3×3 mm^2 including the pixel array, row/column logic, global output buffer, 25 pads, and test structures. The micrograph of the chip and the test board of the proposed temporal-difference sensor are shown in Fig. 8. The sensor operates with a power-supply range between 2.5 and 3 V.

The proposed sensor can provide a light-intensity image as well as a temporal-difference image. Fig. 9 shows the light-intensity image from the fabricated sensor taken under a normal room-light condition and converted to digital data by an external 12-b ADC. The measured fixed-pattern noise (FPN) is 0.3% at 150 lx and 33-ms exposure time, and it is 0.07% at the dark light intensity with the same exposure time. Since the global comparators are used to trigger events, FPN can limit the

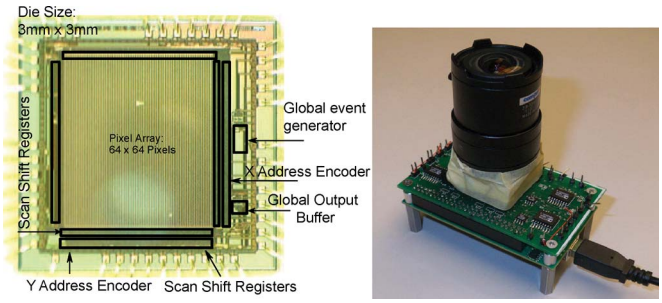

Fig. 8. Image sensor (left) die picture and (right) test board. C-mount lens ($f = 2.8-12$ mm, 1:1.3, 1/3″) is used for the focus.

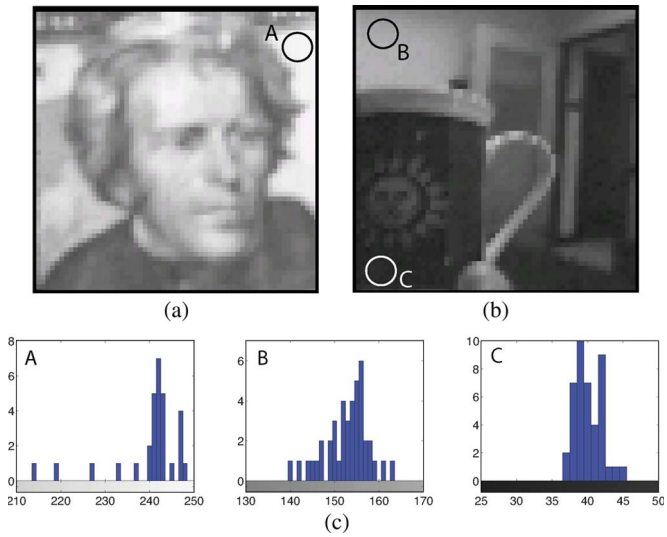

Fig. 9. Light-intensity images from the fabricated sensor. (a) A $20 bill. (b) A cup in an office. (c) Histograms for the dark, middle, and bright regions.

minimum possible threshold voltage. When the measured FPN is 0.3% and the gain is ten, the minimum threshold voltage is limited to around 60 mV for a 2-V pixel signal range.

We tested the performance of the proposed temporal-difference sensor with the following test conditions: the light intensity, frame rate (exposure time), contrast of the input image, comparing threshold voltages, amplification gain, and the speed of the input stimulus. Among the test conditions, the first five test conditions (light intensity, frame rate, contrast of the input image, comparing threshold voltages, and amplification gain) are closely related from a point of view as the input-signal magnitude of the comparator. Therefore, the experimental results were obtained in the same test conditions: 150-lx light intensity, 15-ms exposure time, black and white images (except for the human-movement testing), 0.4-V comparing thresholds, and a gain of ten in the event generator with the same lens (the lens focal length f is 3.7 mm and f-number is 1.3).

Fig. 10 presents the imaging of a spinning object with the proposed temporal-difference sensor. Fig. 10(a) shows the input image, and Fig. 10(b) and (c) shows that the events are generated at the black and white edge. As the speed of the spinning object increases, the number of events also increases linearly. When the speed is about 240 r/min, the mean event rate is about 1700, and the standard deviation is about 170. Since the proposed image sensor uses a rolling shutter readout and

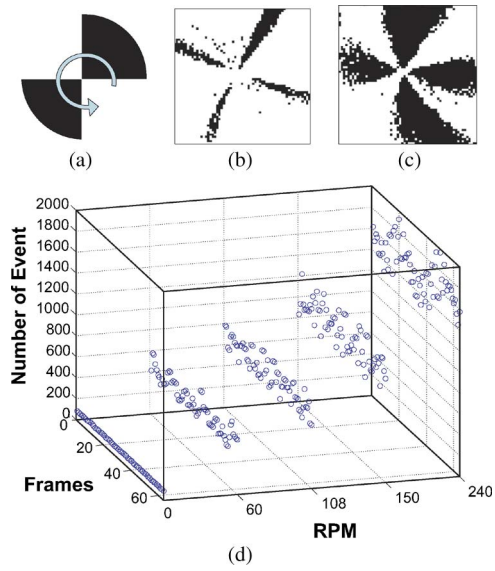

Fig. 10. Measured results with spinning object. (a) Input stimulus image. Event outputs for (b) low and (c) high speed. (d) Distribution of the events.

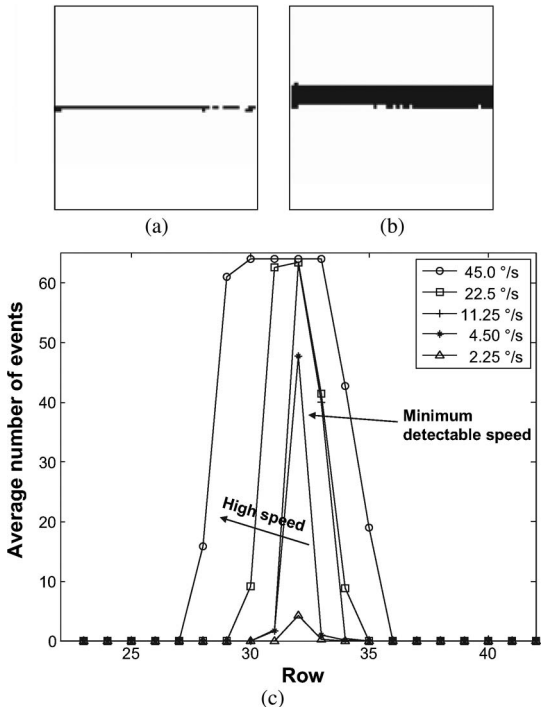

Fig. 11. Measured results with a moving bar at the lens focal length $f = 3.7$ mm. Event outputs for (a) low and (b) high speed. (c) Distribution of the events. The thickness of the event lines is related to the speed of the moving object.

a global high-speed event generator, a motion-blurring effect occurs, as can be seen in Fig. 10(c). Above 240 r/min, temporal aliasing also occurs in the image.

When the movement of the object is slow and the amplified difference is less than the threshold, the proposed sensor cannot generate events. The sensor was also tested with a moving-bar stimulus to measure the minimum detectable speed of the moving object. The thickness of the event lines is related to the speed of the moving object. Fig. 11(a) and (b) shows the AER images and the thickness of the event line at different speeds.

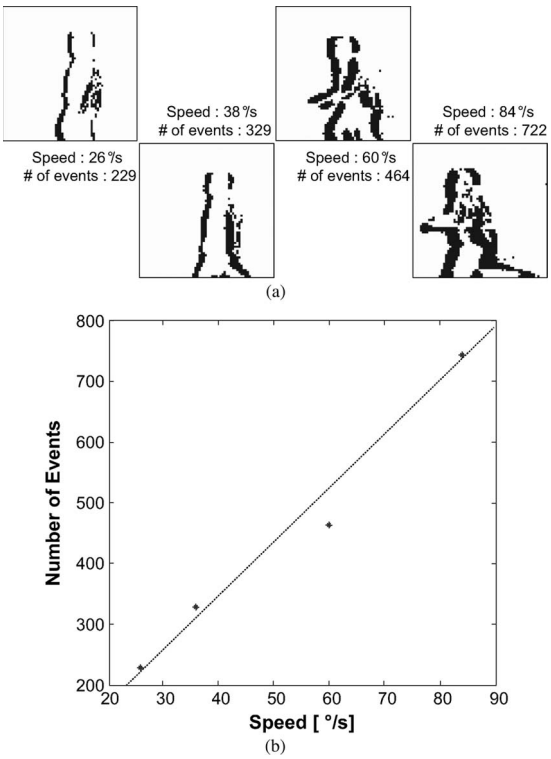

Fig. 12. Measured results with the human movements. The distance between the sensor and the human is 2 m, and the lens focal length f is 3.7 mm.

Fig. 11(c) shows that the thickness of the event line is 4 or 5 pixels at 45 °/s speed, and the minimum detectable speed is 4.5 °/s.

Fig. 12 shows the experimental results with human subjects moving at various speeds. When the human-movement speed is varied from 26°/s to 84°/s (corresponding to slow walk, walk, fast walk, and run), the number of the generated events is from 229 to 722. The linear relationship between the speed of the moving human and the number of the events can be seen in Fig. 11(b) and shows that the proposed sensor can be used for a WSN human-behavior monitoring system [2], [5].

Table I presents the performance summary and comparison of the temporal-difference sensors. The image sensor is capable of computing 30 temporal-difference fps and consumes 1 mW at a power supply of 3 V.

VI. Discussion and Power Analysis of the Proposed Sensor for Sensor-Network Applications

In this section we discuss about the design of a low-power image sensor to achieve long-term surveillance in WSNs. The discussion starts with analysis of the power consumption of the temporal-difference image sensor compared with the power consumption of a COTS imager in wireless sensing applications. Two basic scheduling schemes in the sensor node are discussed to review the tradeoff between detection probability and lifetime in a sensor node platform. The image sensor described in this paper is further investigated with a node platform. Lifetime is estimated at various event rates using simulations when the image sensor is employed in a node platform.

The power-consumption analysis of the proposed sensor is shown in Tables I and II. The measurements were taken when the proposed sensor is running at 30 f/s with a 3-V power supply. The power consumption of the sensor can be divided into four parts: pixel biasing, event generator, output buffer, and digital logic. Notice that the global analog output buffers are the most power-hungry components in the sensor, with 72% of the power consumption. With a current consumption of 355 μA, the proposed sensor can run on two 1155-mA · h AA batteries for 135 days.

In recent sensor-networks research, all the sensor node platforms have chosen a commercially available imager as their visual sensors [17], [18]. However, these COTS imagers are not suited for the sensor-network applications due to the following two reasons.

1) A COTS image sensor consumes tens of milliwatts and blindly collects all visual information, while not considering its usefulness. Collecting video frames and transmitting this redundant visual information not only increase the power budget of the sensor node but also increase the power consumption of the peripheral components used during the wireless communication.
2) The response from a sensor-node's processor is slowed down because much computation and communication resources are required to process redundant visual information. As an example, for transmitting a 320 × 240 visual image of 60 fps at gray scale, the wireless date rate is about 37 Mb/s. The data rate can be reduced to 740 Kb/s when the visual information is represented as AER [1], [2].

In order to alleviate these problems, the sensor-network application needs a low-power AER sensor such as the proposed temporal-difference sensor. There are two basic schemes commonly employed in the scheduling method of the sensor nodes: schedule driven and event-trigger driven. In the *schedule-driven* operation, the sensor nodes are asleep most of the time and periodically wake up to sample for activity [19]. Nodes lose their event-detection probability for power-saving purposes. In the *event-trigger driven* operation mode, a low-power preprocessing unit constantly samples data. It wakes up a more powerful processing unit with an *event* when certain criteria are met [20]. An event-trigger driven scheduling node is capable of keeping a high-detection rate but consumes more power.

The temporal-difference image sensor described in this paper provides a good solution that features an extended lifetime without the sacrifice of detection probability. First, the image sensor samples at 30 fps and the detection rate is constantly kept. Second, the overhead of information preprocessing is 1 mW, which is a hundred times less than a COTS imager. The reduction in the preprocessors' power consumption significantly extends the sensor node's lifetime because the imager keeps the node platform in a deep-sleep mode until significant motion in the scene is detected. The sensor-node lifetime at different event-arrival rates shown in Fig. 1

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF THE TEMPORAL-DIFFERENCE SENSORS

	Proposed	[9] ISSCC'95	[10] ISSCC'05
Pixel Array	64×64	256×256	90×90
Pixel Size	29×28 μm^2	20×20 μm^2	25.2×25.2 μm^2
Technology	0.5μm 2P, 3M CMOS	0.9μm CMOS	0.5μm 2P, 3M CMOS
Pixel Fill Factor	23%	25% without pixel storage	17%
Chip Size	3×3 mm^2	Not available	3×3 mm^2
Dark signal	15mV/s	Not available	Not available
Dark FPN	0.07%	Not available	Not available
FPN	0.4%	1∼2%	0.5%
Operating voltage	2.5∼3V	1.5V	Not available
Frame difference rate	30 frame/s	60 frame/s	30 frame/s
Maximum event rate	129k events/second	Not available	243k events/second
Power consumption	1.06mW	20mW	4.3 mW

TABLE II
POWER-CONSUMPTION ANALYSIS OF THE PROPOSED SENSOR

Component	Current consumption
Pixel biasing	19.2 μA (7%)
Event generator	48 μA (17%)
Output buffer	200 μA (72%)
Digital logic and scan chain	10 μA (4%)
Estimated total current consumption	277.2 μA (100%)
Measured total power consumption at 3 V	1.06mW

was obtained from a MATLAB sensor-node lifetime simulator toolset, which models an iMote2 node's state transition using semi-Markov chain [11]. (The toolset is available at http://www.eng.yale.edu/aspire/matsnl.)

VII. CONCLUSION

We have presented a low-power temporal feature-extracting image sensor for the WSN. The sensor is a 64 × 64 active pixel image sensor with temporal-difference computation capability. The sensor targets low-power image sensing in sensor networks. The sensor computes the temporal-difference between two light-intensity frames and communicates in an address–event format. The chip was fabricated on a 0.5 μm bulk CMOS process and is capable of computing 30 temporal-difference fps while consuming 1 mW at 3 V. The experimental results with various stimuli show that the proposed sensor can be used in the sensor network applications. Intensity image frames are also available at the speed of 60 fps.

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