

A VLSI Neural Monitoring System with Ultra-Wideband Telemetry for Awake Behaving Subjects

Elliot Greenwald, Mohsen Mollazadeh,
Nitish Thakor
Biomedical Engineering Department
Johns Hopkins University
Baltimore, MD 21205, USA
Email: egreenw3@jhu.edu

Wei Tang, Eugenio Culurciello
Electrical Engineering Department
Yale University
New Haven, CT 06511, USA
Email: eugenio.culurciello@yale.edu

Abstract—Long term monitoring of neuronal activity in awake behaving subjects can provide fundamental information about brain dynamics for both neuroscience and neuroengineering applications. Recent advances in VLSI systems has focused on designing wireless neural recording systems which can be mounted on animals and acquire neural signals in real time. These advances provide an unparalleled opportunity to study phenomenon such as neural plasticity in both a basic science setting (learning and memory), and also a clinical setting (injury and recovery). Here we present an integrated VLSI system for wireless telemetry of the entire spectrum of neural signals, spikes, local field potentials, electrocorticograms (ECoG) and electroencephalograms (EEG). The system integrates two custom designed VLSI chips, a 16 channel neural interface which can amplify, filter and digitize neural data up to 16 kS/sec and 12 bits and a low power ultra-wideband (UWB) chip which can transmit data at rates up to 14 Mbps. The entire system which includes these VLSI circuits, a digital interface board and a battery, is small, $1.2 \times 1.2 \times 2.6 \text{ in}^3$, and light weight, 33 grams, so it can be chronically mounted on a rat. The system consumes 32.8 mA at 3.3V and can record for 6 hours running from the 200 mAh coin cell battery. Bench-top and *in vitro* characterization of the system showed comparable performance to the wired recording system.

I. INTRODUCTION

Most studies in basic and clinical neuroscience require wireless transmission of neural signals from the brain to outside world. For example, brain-machine interface (BMI) systems use the neural activity to drive or actuate an outside controller [1], [2]. In the field of clinical neuroengineering, when studying the effects of cardiac arrest on the brain, it is essential to monitor electroencephalographic (EEG) activity to quantify a subject's response to treatment and the following recovery. [3]. However, most of the current recording systems are only capable of sporadic recordings from tethered subjects, making it impossible to correlate the EEG activity to subjects' behavior and outcome. In this field, answering questions as fundamental as, how activity in the brain correlates with survival, requires one of two things. Either a technician must be on call nearly around the clock to continuously monitor subjects, or, researchers must analyze hours of video tape; both

of these solutions are clearly economically sub-optimal. These challenges require significant technological progress to able performing experiments in untethered, awake and behaving animals. These systems could be transformative in the same way that multi-electrode arrays ushered in a paradigm shift in systems neuroscience research [4].

Recently, there has been a significant amount of work focused on designing systems which can record neural activity in awake behaving subjects [5]–[7]. Wireless modalities such as bluetooth, frequency-shift-keying, and ultra-wideband pulse radios have been explored. Hampson *et al.* [8] reported on a custom built system with bluetooth technology which can transmit 16 channels of neural data from awake and freely moving rats. This system achieved a transmission rate of around 150 Kbps, and could record for over five hours when powering their system from a 40 gram battery pack. Another group designed their system to log data onto a flash memory card, bypassing the need for a wireless transmitter [7]. In fact, a later incarnation of the same system [9], reported on a design which employs a separately described custom neural recording VLSI chip with on-board FSK telemetry [10]. This system was mounted on a rhesus monkey, and used to record neural activity continuously for six days. One channel of neural data was sampled at approximately 16 Kbps, and wirelessly transmitted. Lastly, ultra-wideband wireless technology is also being explored since it offers both high data rate and low power consumption. Chae *et al.* [11], recently reported on a 128 channel neural recording IC with an on-board UWB transmitter capable of transmitting data up to 90 Mb/s. This system was tested on excised snail neural tissue and offered on board spike sorting - emphasizing the ability to perform digital signal processing alongside analog acquisition and RF telemetry.

Although the above systems offer great performance in recording neural responses, they do not offer either lower weight or low power consumption. Here we present an integrated neural recording system for monitoring neural activity from rats. The system comprised of of two previously reported

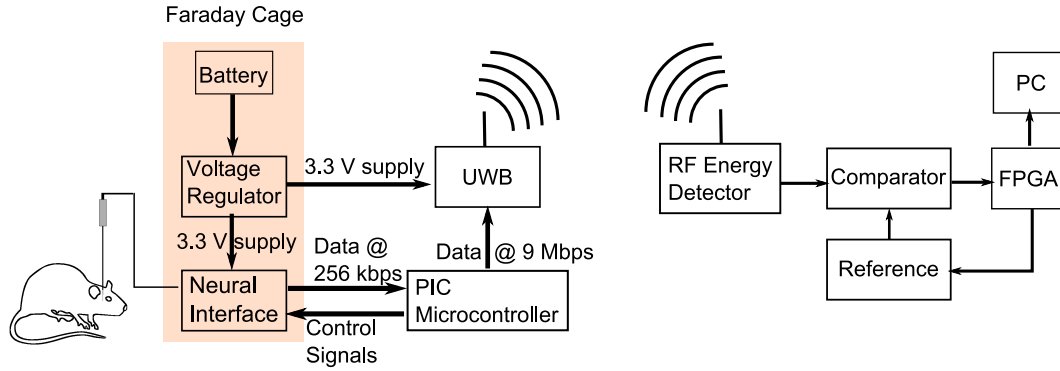


Fig. 1. A functional block diagram of the developed system: Neural signals are amplified, filtered and digitized by a custom designed VLSI chip. Then a microcontroller packages the data and send it to a VLSI ultra-wideband transmitter. Signals are received using a commercially available RF detector and read into the computer using an FPGA-USB interface.

custom integrated circuits, that together comprise a wireless neural monitoring system. Section II describes the functional and physical design of the system, section III contains experimental results, and section IV concludes the paper.

II. DESIGN

The ultimate goal of the proposed system is to enable monitoring of neural activity in awake behaving rats. It is important that the system burden the animal; otherwise, it could alter its behavior, thus defeating the whole purpose of recording in an awake animal. Assuming that the target subject can carry 15% of its weight, the proposed system should be below 40g. Also, the system's total volume must be constrained such that it does not hinder the movement of a subject's limbs. For long term monitoring it is only necessary to transmit the data from an animal's cage, to a nearby computer. The system therefore needs an operational distance of at least 1 m. These constraints require the system to be ultra-low power with a miniature footprint while maintaining comparable performance to the wired recording systems. To this end, we have designed a system which meets the above requirements in bench-top testing. The proposed system is composed of a 16-channel VLSI neural interface chip, an UWB telemetry VLSI chip and a digital interface unit which controls the operation of the VLSI circuits and data communication between them. Power is delivered via a coin-cell lithium-ion battery and regulated. Fig. 1 illustrates the block diagram architecture of the system, summarizing the important components, and their connections.

A. Neural Front-end

The 16 channel neural interface system was designed in 0.5 μm 2P3M process and occupied 3 mm by 3 mm of silicon area. Each channel of the neural front end contains a bandpass amplifier with tunable bandwidth and a programmable $\Delta\Sigma$ ADC. The bandpass amplifier in the front-end offers fixed gain (40 dB) amplification with tunable lowpass filtering from 140 Hz to 8.2 kHz. The bandpass amplifier was designed using a two stage fully differential amplifier with independent common mode feedback circuitry (CMFB) in each stage. Each neural amplifier offers a $3 \mu\text{V}_{rms}$ input-referred noise for the

1-140 Hz bandwidth while drawing 300 μA of current from the power supply. The amplified neural signal is then digitized using a configurable incremental $G_m - C \Delta\Sigma$ ADC. This ADC offers programmable resolution from 8 to 12 bits and digital gain of 1 to 4. The digitized output is then read out using a parallel-in serial-out shift register. A detailed description of this system can be found in [12].

B. UWB Telemetry

The UWB circuit was fabricated in the 0.5 μm silicon-on-sapphire (SOS) process and occupies $420 \mu\text{m}$ by $420 \mu\text{m}$ of silicon area [13]. The integrated transmitter consists of a voltage controlled ring oscillator as the compact pulse generator and an output buffer as the modulator. The transmitter is capable of generating pulses with 1-ns width and the pulse rate can be controlled between 90 MHz and 270 MHz. The data rate of this wireless link can reach a maximum of 14Mbps. This UWB chip can provide the wireless link in the 3-4 meters range while consuming 10-20 mW of power from 3.3 V supply. The system was tested with a 2 by 1.5 in triangular antenna which was mounted on the same PCB as the UWB chip.

C. System Integration and Packaging

Fig. 1 illustrates the high-level block diagram architecture of the system. The animal under study represents the first stage in this system. Electrodes implanted in its brain interface with the neuropotential VLSI chip which amplifies and digitizes the EEG from rat cortex. The digitized data from all 16 channels are then shifted out serially, and received by a PIC microcontroller (PIC24HJ64), which also programs the digital gain and resolution of the neuropotential chip, and several biases set by a digital to analog converter at power-up. Each 12 bits are written to a word long memory location, and a header of '0101' is appended to the data from each channel to help decode the data at the receiving end. Once eight words are acquired by the PIC, it sends the data to the UWB chip through the serial peripheral interface (SPI) port at a rate of 9 Mbps with a 16 bit header appended to the whole package. We have chosen this PIC since it offers direct memory access (DMA), and an idle mode, in which current consumption drops

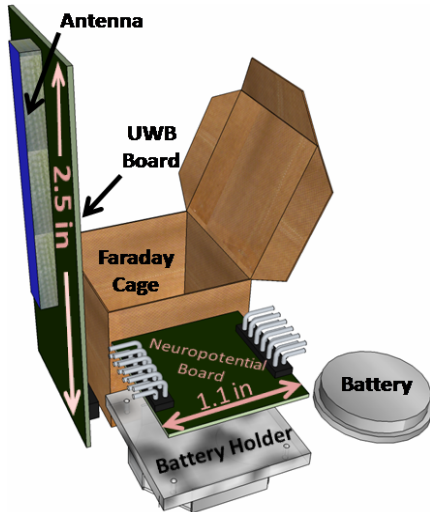


Fig. 2. A three dimensional model of the system: The neuropotential board, the battery pack and the battery all fit in the faraday cage. The UWB board connects through an incision in the Faraday cage (not shown).

to about 6 mA while peripherals such as the DMA and SPI continue to operate. The transmission of data from SPI port to the UWB is achieved by the direct memory access module (DMA) on the PIC. Hence the read in operation of new data is not interrupted by the transmission of old data.

At the receiver side, an RF detector (Analog Devices, ADL5519) reconstructs the energy envelope from the impulse sequences and the output is digitized through comparison with a tunable reference voltage which is set by a digital to analog converter (AD7398). The digitized data is read into an FPGA (Xc3s1000), which waits to receive the 16 bit header for the package. Once the header is detected, the FPGA reads the eight channels worth of data, and stores it in an on-board DRAM which acts as a buffer. The data is then transferred to a computer and displayed in real-time with custom software written with LABVIEW (National Instruments, Austin, TX). The computer has access to the FPGA through a USB interface designed by Opal Kelly (Xem3010).

The physical design of the system is shown in Fig. 2. The neuropotential chip is wire-bonded to a 1.1 x 1.1 in² printed circuit board. This board also contains a voltage regulator, and a digital to analog converter plus four potentiometers to supply bias currents to the neuropotential chip.

The battery power supply is stacked below this board using four screws. These two components fit in a 1.3 in³ Faraday cage made from a 0.0045" diameter copper wire mesh. The fine mesh is grounded, and shields the amplifiers and ADC from the high frequency noise of the transmitter.

The transmitter and microcontroller board are assembled on one PCB and are external to the Faraday cage. A set of vertical headers connect this board to the neuropotential interface board. We currently use a commercial surface mount antenna (FR01-B1-S-0-047), diagramed in the 3-D model in blue.

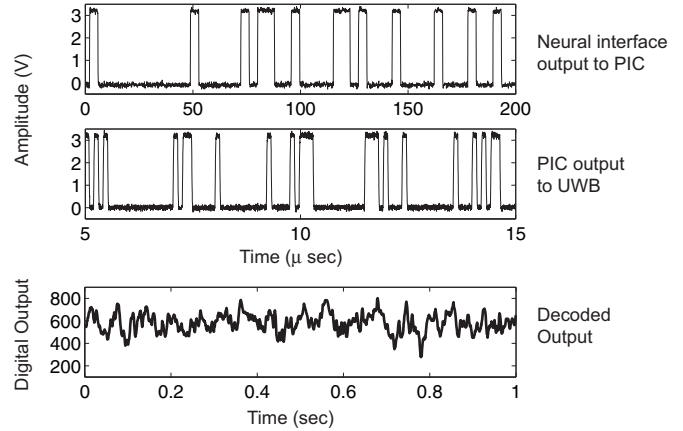


Fig. 3. Oscilloscope traces of outputs from the neuropotential chip to the PIC (top), the PIC to UWB module (middle), and the decoded trace of a prerecorded EEG waveform, recorded through a saline solution. Note the difference in time scales: the neuropotential chip shifts data out at 256 kHz, the PIC shifts data out at 9 MHz, while the transmitted waveform had most of its frequency content around 20 Hz.

D. Power Supply

Power is supplied to these circuits with a 3.7 V, 200 mAh rechargeable Li-Ion coin cell battery (Korea Power Cell, PD2450). Both the neural recording board and the transmitter board have are equipped with low drop-out 3.3 V regulators (Texas Instruments, TPS7233). In choosing a battery, a significant tradeoff was made between power and size/weight. While small and light weight Li-Ion batteries are becoming ubiquitous, we limited the size of our battery by the size of the neuropotential board, 1.1 inches maximum in any direction. Additionally, we ruled out any battery weighing more than 10 grams. The battery used in this design has a diameter of 1 inch and weighs 6 grams.

III. RESULTS

The described system was assembled and packaged; the neural interface and battery reside in a 1.2x1.2x0.9 in³ Faraday cage, while the transmitter sits outside on a 1.1x2.6x0.06 in³ PCB. Benchtop testing was performed with the system. Since the neural interface circuit and UWB chip has been individually characterized and reported before, we only focus on the system level performance of the whole design. Briefly, the neural amplifier had a midband gain of 39.6 dB and was configured for a bandwidth of 1 kHz to perform recording in rats. The ADC digital gain and resolution was set to 1 and 10bits respectively. With these settings, each neural channel offered 2.5 μV_{rms} input-referred noise while consuming 22 μA of current from the 3.3 V supply. A 1 mV_{pp} 25 Hz sine wave was generated (not shown), fed into the neural interface chip, and transmitted. The received signal had a THD of less than 1% and a SNR of 55 dB. A bias was provided to the UWB module such that it operated with its maximum pulse repetition rate of 270 MHz; the chip consumed 8 mA of current.

The neural recording system draws 32.8 mA of current from the battery. In this configuration, we have measured that the system can run continuously for approximately 6 hours. Both these recording periods are sufficient to perform neural monitoring in rats. The total weight of the packaged system is 33 grams which meets our criteria of 15% of body weight for medium to large sized rats.

Fig. 3 shows the result of benchtop characterization of the system. The neural recording board was interfaced to a phosphate buffered saline (PBS) solution while prerecorded EEG data from rat somatosensory cortex was played into the PBS using a function generator (Agilent Technologies). The neural interface bandwidth was set to 1 kHz and the amplified signal was digitized to 10 bits. The top trace of Fig. 3 shows the asynchronous digital output from the neural interface chip at 256 kbps. The middle trace of Fig. 3 shows the output from the PIC to the UWB module which is transmitted at a rate of 9Mbps (note the difference in time scale). The decoded and reconstructed EEG signal is shown in the bottom trace of Fig. 3. The received signal closely matches the original waveform.

As a final note, the upper limit on the data rate is set by the choice of microcontroller rather than the transmitter/receiver pair. As mentioned earlier, data is sent out to the UWB from the PIC's SPI port. This peripheral has a maximum data rate of 10 Mbps, which sets the upper bound for our systems data rate, the UWB system we employ, described in [13], is capable of transmitting at speeds up to 14 Mbps. Table I summarizes the performance of the system.

IV. CONCLUSION AND FUTURE WORK

We have presented a small, light-weight, and low-power stand-alone VLSI recording system with ultra-wide band telemetry for monitoring neural activity in awake behaving subjects. The system weighs 33 grams and consumes 32.8 mA of current from 3.7 V battery. The system can record from up to 16 channels of EEG, ECoG, or spikes, and can transmit data at rates up to 10 Mbps. We successfully performed benchtop as well as *in vitro* operation of the system.

Our future work focuses on recording neural signals from awake behaving rats following cardiac arrest. This system will present us with the opportunity to better understand the consequences of injury to the brain and neural signatures of arousal and recovery in EEG signals following treatment such as hypothermia [3]. Moreover, a second generation of the neuropotential chip will be developed to address issues of size, power consumption, and robustness. These changes will include the generation of the required biases on chip. This slight change would substantially bring down the size of the neuropotential board's footprint. We will also modify the current UWB system design in order to increase both the data rate, and the transmission distance of the system.

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TABLE I
PERFORMANCE SUMMARY OF THE SYSTEM

| | | | |
|------------------|---|-----------------------------|-----------------------|
| Neural Interface | Gain | 39.6 | dB kHz |
| | Bandwidth | 0.14 - 8.2 | |
| | THD , $v_{in} \leq 9.4mV_{pp}$ Noise Efficiency Factor | < 1% < 3 | |
| UWB | Max Data Rate | 14 | Mbps nJ/bit mW |
| | Energy per Bit | 1.5 | |
| | Pules Generator Power Consumption | 0.6 | |
| | BER @ 1m | 10^{-4} | |
| System | Number of Channels | 16 | mA grams in^3 |
| | Current Consumption | 32.8 | |
| | Weight | 33 | |
| | Volume | $1.2 \times 1.2 \times 2.6$ | |

and Jay Burns for his help in building the Faraday cage. Chips were fabricated through the MOSIS foundry service. This work was supported by NIH MH062444-065296, ONR 439471 and 396490 and NSF 06493449 grants.

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