4-Channel Asynchronous Bio-potential Recording System

Wei Tang, Chenxi Huang, Dongsoo Kim, Berin Martini, Eugenio Culurciello
Electrical Engineering Department, Yale University
New Haven CT 06520
{eugenio.culurciello, wei.tang}@yale.edu

***Abstract*— We present a 4-channel bio-potential recording system using asynchronous delta analog-to-digital converter. The system is designed to reduce the amount of data in neuro-physiological sensors. The circuit includes low-power low-noise amplifiers with asynchronous delta modulators. The analog front end offers a gain of 53dB within bandwidth of 200Hz-20kHz. In this asynchronous data converter, the minimum input-referred delta resolution is 4μV. The input-referred rms noise is 2μV. The system was fabricated with AMI 0.5μm CMOS technology. The chip size is 1.5mm by 1.5mm. The power consumption of the 4-channel system with 3.3V supply is 118.8μW in static state and 501.6μW with 240kbps data conversion rate. A graphic user interface was developed to monitor the transmitted signal in real time.**

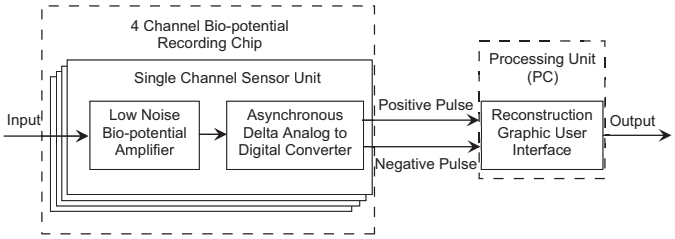

Fig. 1. Block diagram of the amplifier and signal conversion system. The input neural signal is amplified and modulated to digital pulse sequence by asynchronous delta modulator. A graphic user interface (GUI) reconstructs the waveform based on the digital pulse sequence and threshold voltages.

I. Introduction

There is a growing need for bio-potential recording systems to monitor neural activity for neuroscience and clinical experiments [1]. The challenges of neural recording systems are the power and data constrains. The system power consumption should be limited in order to avoid heating damage to the tissue. Another constrain is that the speed of commercial wireless devices is not sufficient to communicate the large data streams from the bio-potential recording array [2]. These problems can be attributed to traditional synchronous sampling and conversion methods [3] operating at fixed Nyquist rate. When recording neural signals, only the data from spike pulses is of interest. Constantly sampling the neural signal wastes the sampling bandwidth and increases the data rate of the communication circuit.

To solve this problem, in this paper we present a design that employs an asynchronous level crossing sampling technique. By using this method, the data converter is active only when the signal is changing. The output of the sensor is digital, and the data rate is highly reduced due to the nature of the sparse spikes of the bio-potential signal. The asynchronous delta analog-to-digital (A/D) conversion only executes amplitude domain quantization but leave the time domain quantization to the receiver part. The circuit power consumption is reduced observably. Moreover, as the A/D conversion circuit works asynchronously, the system is free from the noise interference by the fixed-sampling-rate clock.

The main contribution of this paper is the implementation of a novel high resolution asynchronous delta modulation circuit for the bio-potential measurement system. An on-chip asynchronous delta modulator was designed to perform amplification and A/D conversion. The delta step resolution is 2mV while the output swing of the 53dB amplifier is 2.2V. The equal minimum input-referred delta resolution is 4μV. This system is capable of reducing the data size up to 960 times [4] while keeping the resolution of the analog to digital conversion. The power consumption of the circuit is suppressed to 125.4μW in each channel at 60kbps data rate.

II. System and Circuit Design

The block diagram of the asynchronous bio-potential recording system is illustrated in Fig. 1. The system contains a reconstruction graphic user interface and a 4-channel bio-potential recording integrated circuit. The on-chip recording circuit has a low-power low-noise bio-potential amplifier and an asynchronous delta modulation circuit. When the input signal increases or decreases by a fixed threshold (as the positive delta and negative delta), the asynchronous A/D conversion generates a pulse to reset the delta modulator. By doing so the output of the amplified signal is converted to positive and negative pulse sequences and sent to the processing unit (on computer). The pulse rate is directly proportional to the rate of the signal change.

Reconstruction of the pulse streams is performed by a data sequence in the computer. According to the timing of the positive and negative pulses, the value in the data sequence is increased by a positive delta with each positive pulse, and decreased by a negative delta with each negative pulse. Plotting the data sequence over time reconstructs the original signal. In the asynchronous A/D conversion, the signal is sampled only when it changes. Accumulation of the offsets can be removed from the data collecting program by the computer.

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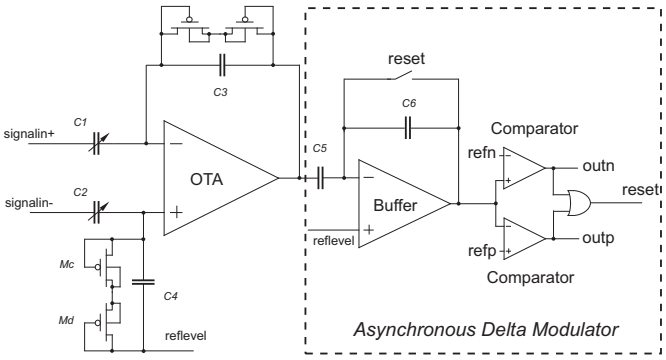

Fig. 2. Schematic of the bio-potential recording chip. The capacitor feedback of the amplifier is designed to filter out the DC component of the input signal while rejecting common-mode noise. *C1* and *C2* are tunable capacitors for changing the gain. The MOS-bipolar pseudoresistor elements are working as large resistors to amplify low frequency signal and reject the DC offset. The amplified analog signal is compared with the threshold voltages. When the comparator triggers, a digital pulse is send to the output and the delta modulator is reset.

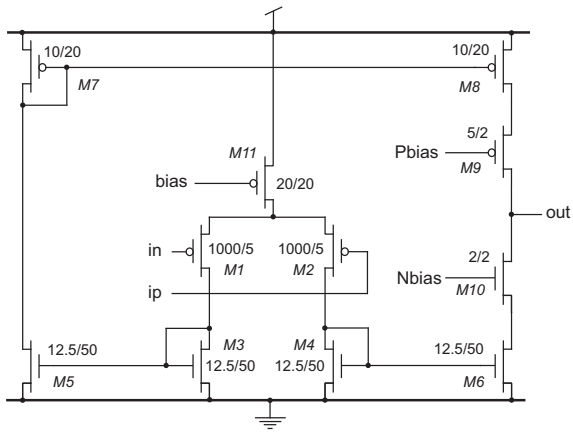

Fig. 3. Schematic of the low-power low-noise operational amplifier (OTA) with the sizes (W/L ratio) of the devices. The input stage is a PMOS pair to reduce noise. The output stage is a cascade amplifier to increase the gain.

The design of the integrated circuit contains the amplifier and delta modulation A/D circuit, which is shown in Fig. 2. A low-power low-noise operational transconductance amplifier (*OTA*) [5] is used as the main amplifier. Capacitor feedback is designed to work with the *OTA* to reject DC variation of the neural signal. The bandwidth of the design is 200Hz-20kHz. *Ma-Md* are utilized as large pseudoresistors to amplify low frequency signals and reject DC offsets. In the feedback, *C1* and *C2* are tunable capacitors, which can be selected to 7pF or 35pF. *C3* and *C4* are 50fF.

A high speed unit gain buffer follows the main amplifier in order to perform resetting in the delta modulator. The delta modulation is carried by an asynchronous reset signal. Two threshold voltages are compared with the buffer output. The gap between the threshold voltage (*refn* or *refp*) and signal ground (*reflevel*) is the positive or negative delta. If the amplifier output is larger than the positive threshold or smaller than the negative threshold, the comparator output will set to logical high. The high *reset* output will reset the buffer output to signal ground. After reset, the outputs of the comparators will be logic low as the signal ground is in the window between the two threshold voltages. Then the reset signal is released to make the buffer return to the follower mode automatically. After reset, a voltage difference between the amplifier output and signal ground might exist, but this difference will be considered as DC difference and hence can not pass the buffer. This process will generate a pulse from one of the comparator output (*outn* or *outp*). The comparator output is the result of the pulse-based A/D conversion. The self-reset scheme makes the circuit a clock-less A/D converter.

The previous design [4], because of the small bandwidth (200Hz-20kHz) of the low-noise high-gain bio-potential amplifier, when the amplifier is included in the modulator loop, the response time of the modulator (output pulse width) is long (350ns), hence the delta step can only reach to 0.1V, which is not small enough to meet the resolution requirement. In this improved design, a faster buffer is used to perform the reset. The pulse width is reduced to 30ns and the delta step is reduced to 2mV.

The schematic of the *OTA* is shown in Fig. 3. The bias current of M11 is set to 5μA and current in M1-M10 is 2.5μA. A cascade structure is used in the output stage to boost the gain. The circuit is designed to suppress noise while maintaining relevant speed for neural signal processing. The W/L ratio of the input differential PMOS transistor pair is large (1000μm/5μm) to reduce input referred noise. The intrinsic gain of the OTA is 94dB. A high-performance comparator [6] including preamplifier, decision circuit and output buffer is implemented. The schematic of the comparator is shown in Fig. 4.

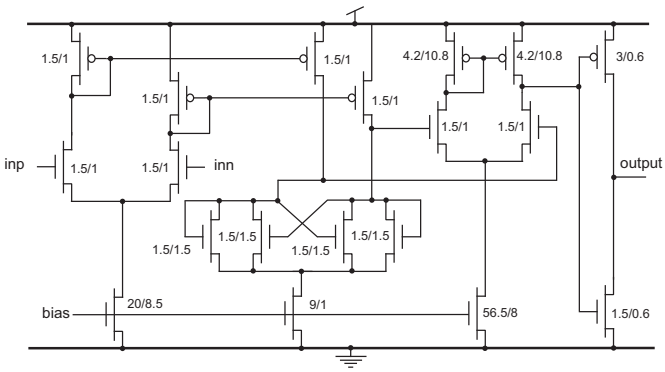

Fig. 4. Schematic of the comparator with the sizes (W/L ratio) of the devices, including preamplifier, decision circuit and output buffer.

III. Experimental Results

The circuit was fabricated using AMI 0.5μm 3M2P process. The feed back capacitors are build of PIP (polysilicon-insultor-polysilicon) structure. The measured gain of the bio-potential amplifier is 53dB between 200 and 20kHz. In this bandwidth, the input referred noise is 20nV/$\sqrt{Hz}$ with rms of 2μV. The input-referred noise is calculated from the measured output

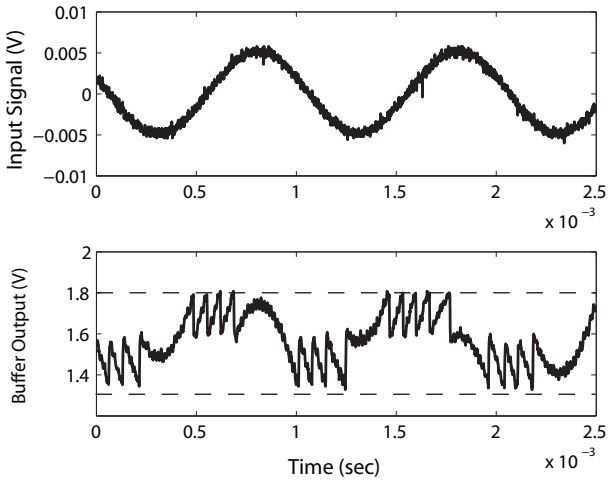

Fig. 5. Measured chip input and output waveform in 3.3V single power supply. Top: 1kHz input signal with amplitude of 10mV. Bottom: Analog front end output signal with delta modulation. The positive threshold is 1.8V and negative threshold is 1.35V. Signal ground (*reflevel*) is 1.65V.

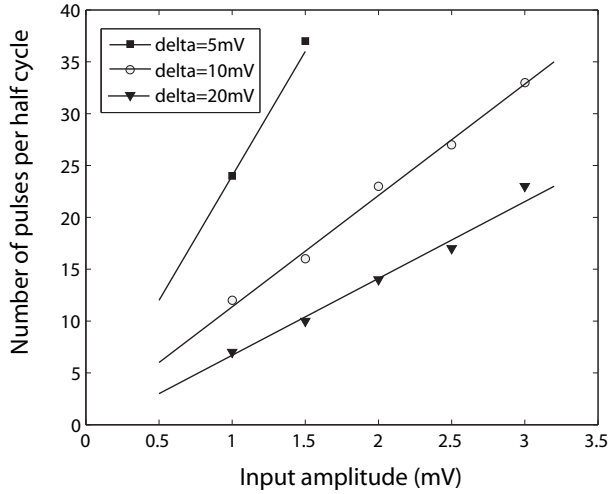

Fig. 6. Measured linearity of delta modulation. The input signal is 1kHz sine wave. The number of the pulses when input signal changes from peak-to-peak (half cycle in sine wave) is proportional to the input signal amplitude.

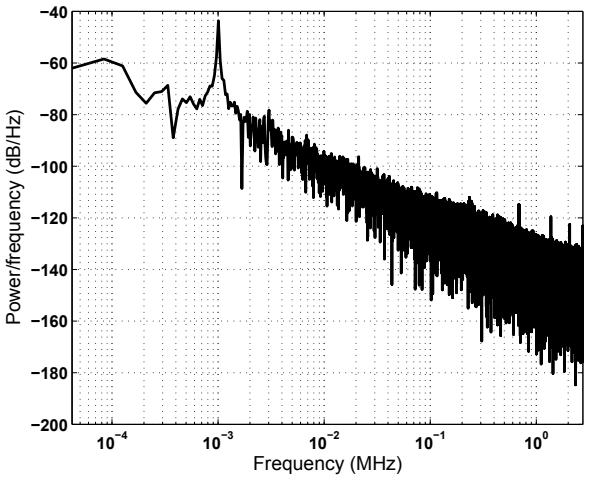

Fig. 7. Power spectrum density of the reconstructed waveform. The input signal is a 1kHz sine wave with 6mV peak to peak amplitude.

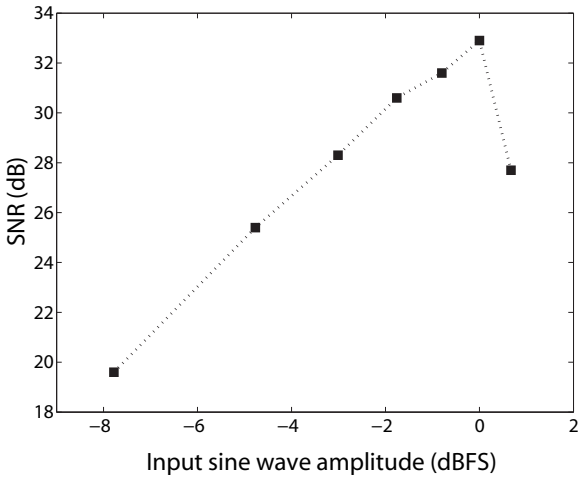

Fig. 8. Measured signal to noise ratio of the delta modulator as a function of input signal amplitude. The amplifier is saturated if the input signal is more than 7mV. The 0 dBFS refers to 6mV full scale input amplitude

noise and amplifier gain. The experiment results shows that the cross talking between channels can be ignored.

Fig. 5 shows the measured input and output waveform of the amplifier and data conversation circuit. The input signal is a 1kHz 10mV peak-to-peak sine wave. Referring to Fig. 2, the buffer output signal is compared with the positive (1.8V) and negative (1.35V) threshold voltages. If buffer output exceeds the window between the two threshold voltages, the buffer will be reset to the signal ground. During the reset mode, the comparator generates a digital pulse. An OR operation of the two pulse sequences from comparators will produce the asynchronous reset signal for the delta modulation, shown as *reset*.

The linearity of the delta modulation has been measured and illustrated in Fig. 6. We use a 1kHz sine signal as the input signal and set the delta step to 2mV, 10mV and 20mV, then count the number of pulses in *reset* while the input changes from peak to peak (half cycle of the sine wave). When the delta step is fixed, the number of the pulses are linearly proportional with the input signal amplitude.

The power spectrum density of the reconstructed sine waveform is plotted in Fig. 7. The measured signal to noise ratio is 34dB in the interested bandwidth. The low frequency noise is generated during reconstruction and can be removed easily by software.

The signal to noise ratio of the reconstructed waveform as a function of the input signal amplitude is shown in Fig. 8. The 0 dBFS is the 6mV full scale input amplitude. The measured SNR is smaller than ideal case because of the finite loop delay time of the delta modulator.

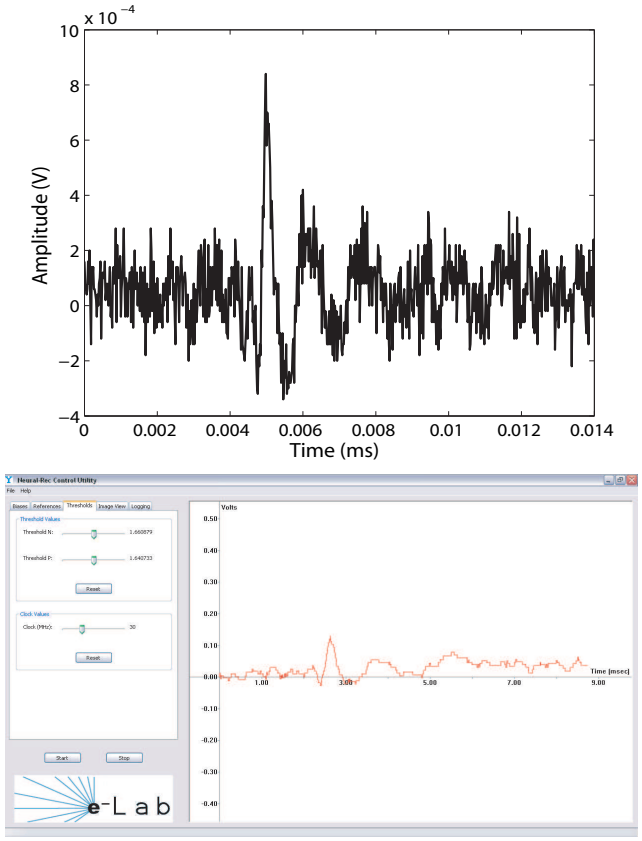

Fig. 9. Reconstructed waveform in GUI, running in real time. Top: neural signal from a rat barrel cortex. Bottom: reconstructed waveform in GUI.

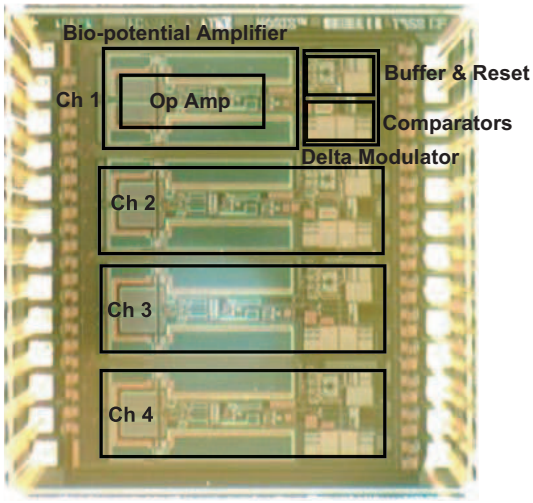

Fig. 10. Chip micrograph with main building blocks highlighted.

Process technology	AMI 0.5μm CMOS
Chip size	1.5mm by 1.5mm
Supply voltage	3.3V
Amplifier Bandwidth	200Hz-20kHz
Amplifier Gain	53dB
Amplifier Output swing	2.2V
Input-referred rms noise	2μV
Amplifier power	75.9μW
Chip power (4-channel static)	118.8μW
Chip power (pulse rate 240k/sec)	501.6μW

TABLE I
SUMMARY OF THE CHIP CHARACTERISTICS.

A demo system is developed using an OpalKelly 3001v2 FPGA as the interface between the chip and PC (GUI). In the system, the pulses are sampled and sent to the PC, where the output waveform is reconstructed by adding or subtracting the delta amplitude according to the pulse sequences. The amplitude of the delta step can be controlled from the GUI via a 12 bit DAC (AD7398). The system is running in realtime for monitoring the activities of the input signal. The reconstructed waveform of a real neural signal from a rat barrel cortex is displayed in the GUI as shown in Fig. 9. The spike is 1mV amplitude and 0.6ms duration. The delta amplitude of the system is set to 2mV.

IV. Summary

We designed and tested the fabricated 4-channel low-power low-noise for bio-potential recording system. The chip micrograph is illustrated in Fig. 10. The chip area is 1.5mm by 1.5mm. Table I summarizes the main properties of the chip. The test result shows that our circuit consumes 118.8μW in statical mode and 501.6μW when the pulse rate is at 60k/sec (60kbps data rate) in each channel (total 240kbps). The system provides remarkable data reduction, clock-less A/D conversion and low power consumption. This design is a competitive solution in neural recording system.

V. Acknowledgements

This project is funded by ONR grant number 439471 and 396490, and NSF award 0649349. The support of MOSIS in chip fabrication is gratefully acknowledged. We also thank Berin Martini for the help in the GUI development, and Selcuk Talay for the help in the chip measurement.

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