An Integrated Patch-Clamp System with Dual Input

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***Abstract*—We present the first, fully integrated, multi-channel implementation of a patch-clamp measurement system. The system was implemented in a 0.5 μm silicon-on-sapphire process. The system can record two simultaneous cell membrane currents up to $\pm$20 μA with a rms noise of 8 pA in a 10 kHz bandwidth. The system can compensate for the capacitance and resistance of the pipette electrode, up to 10 pF and 100 MΩ respectively. The system die size is 3 x 3 mm and the power consumption is 5 mW per channel at 3.3 V.**

I. INTRODUCTION

Patch-clamp is the electrophysiology gold standard technique to measure ion-channel currents of cells when the cell membrane is "clamped" to commanded voltages. The patch-clamp technique reports the highest signal-to-noise ratios available in amperometric cell measurements, but is slow and labor-intensive when performed manually [1]. We present a multi-channel integrated patch-clamp amplifier, an enabling technology along with planar electrodes to perform simultaneous and automatic measurements on a large number of cells in parallel for high-throughput electrophysiology [2].

The systems was implemented in a 0.5μm silicon-on-sapphire (SOS) technology for its linear, high-value resistors needed to implement R_f. The insulating substrate in SOS also minimizes the cross talk between channels [3], [4]. The device is a fully integrated, 2-channel system miniaturized in a 3 x 3 mm^2 silicon area, 10 million times smaller in volume than commercial bench-top systems.

II. PATCH-CLAMP SYSTEM OVERVIEW

Fig. 1 shows a block diagram of the integrated 2-channel patch-clamp system (right) and the electrical model of a cell and pipette electrode (left). Multiplying digital to analog converter mDAC 1 controls the parasitic capacitive compensation, mDAC 2 provides leak subtraction, mDAC 3 and the phase-lag controller circuit provides series resistance compensation. Input reconstruction and output anti-aliasing filters are also integrated.

In whole-cell patch recording, a pipette filled with a saline solution is used to adhere to the cell. Cells are stimulated by applying voltage steps across the cell membrane (V_p = V_{clamp}). After applying compensation, the circuit then measures the resultant ion-channels current I_i. The cell membrane can be modeled as a capacitance C_m in parallel with the membrane resistance R_m.

The system compensates for the difference between the actual membrane voltage V_m and the clamping voltage V_{clamp} due to the voltage drop across the pipette electrode series resistance R_S. The circuit also compensates for the current i_{prs} drawn by the electrode parasitic capacitance C_{prs}. The headstage of the patch-clamp recording system consists of a current-to-voltage transimpedance amplifier that uses resistive feedback (with a user-selectable R_f). A difference amplifier subtracts V_{clamp} from the transimpedance output. The resultant output voltage V_{out} is proportional to the input current, I_{in}.

III. ELECTRODE COMPENSATION CIRCUITRY

The drop across R_S is compensated by adding a fraction of V_{out} to the applied membrane-command potential V_{com} using a positive feedback loop to obtain V_{clamp}. A phase-lag compensation circuit was added to the positive feedback loop to improve stability when a higher percentage of R_S is compensated. R_S compensation is necessary for two reasons. First, it allows accurate voltage clamping of the membrane by bringing V_{com} closer to V_m. Second, the technique reduces the time needed to charge C_m enabling the circuit to monitor ion-channel events occurring immediately after V_{com} is applied [5]. The parasitic electrode capacitance C_{prs} is compensated by injecting a current i_{inj} through an integrated capacitor C_{inj} of 10 pF. Parasitic capacitance compensation prevents the saturation of the headstage by eliminating high-amplitude, high-speed, capacitive overshoots. The removal of these parasitic overshoots is also essential to guarantee the stability of the positive feedback loop of the resistive compensation circuit. Any instability in the circuit can cause irreversible damage to the cells under test. The leak compensation circuit subtracts leak currents when recording with low seal-resistances. Compensation circuits are addressed with a digital control word applied to the mDACs to vary the amount of compensation.

IV. HIGH-PERFORMANCE OPERATIONAL AMPLIFIER DESIGN

A low-noise, rail-to-rail, constant-transconductance operational amplifier was designed for the system to measure ion-channel currents with high fidelity. Rail-to-rail operation of the amplifier is needed to allow large V_{com} with high R_S compensation and to improve the signal-to-noise ratio of the system. Constant transconductance is needed to perform linear

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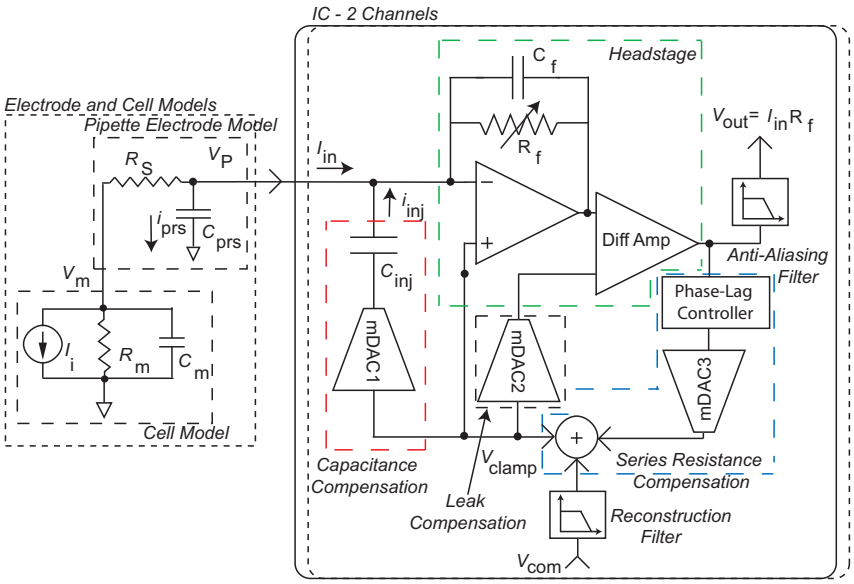

Fig. 1. The integrated 2-channel patch-clamp system (right) and the electrical model of a cell and pipette electrode (left). Multiplying digital to analog converter mDAC 1 controls the parasitic capacitive compensation, mDAC 2 provides leak subtraction, mDAC 3 and the phase-lag controller circuit provides series resistance compensation. Input reconstruction and output anti-aliasing filters are also integrated.

compensation protocols over the entire rail-to-rail, common-mode range. Fig. 2 shows a schematic of the operational amplifier used in the design.

V. Measurement Results from the Patch-Clamp System

Fig. 3-A shows the measured step responses of the series resistance compensation circuit. The time constant τ associated with charging the membrane capacitance $C_{\rm m}$ through a compensated resistance ($R_{\rm S}$-$R_{\rm comp}$) when a step $V_{\rm com}$ is applied (inset), is given by $\tau = (R_{\rm S}\text{-}R_{\rm comp})\times C_{\rm m}$. Increasing compensation, $R_{\rm comp}$ approaches $R_{\rm S}$ and τ decreases, increasing recording bandwidth. Using the series resistance compensation circuit, we were able to compensate a 4 MΩ electrode series resistance, decreasing the time needed to charge $C_{\rm m}$ from $\tau = 200\mu$s to 50μs (75% compensation) and 120μs (100% compensation with phase-lag). The effect of parasitic capacitive compensation is shown in Fig. 3-B. When uncompensated, the headstage provides the current $i_{\rm prs}$ needed to charge the parasitic capacitance. This current appears as overshoots in the current monitoring signal with the same polarity as $V_{\rm com}$. When properly compensated, $i_{\rm prs} = i_{\rm inj}$ and the overshoots do not appear. When overcompensated, $i_{\rm inj} > i_{\rm prs}$ and the overshoots appear negative.

Fig. 4-A shows the rail-to-rail performance of the operational amplifier used in the design. Here a 1 kHz sine wave is presented to the amplifier in follower configuration with a 15 kΩ load. Fig. 4-B reports the constant gain-bandwidth product (which implies constant-transconductance) of the amplifier over its input common-mode range [6]. The measured input-referrd offset voltage and slew rate were 0.4 mV and 10 $\frac{V}{\mu s}$ respectively. The measured input-referred voltage noise of the operational amplifier was $3\times10^{-9}\frac{V}{\sqrt{\rm Hz}}$ at 10 kHz.

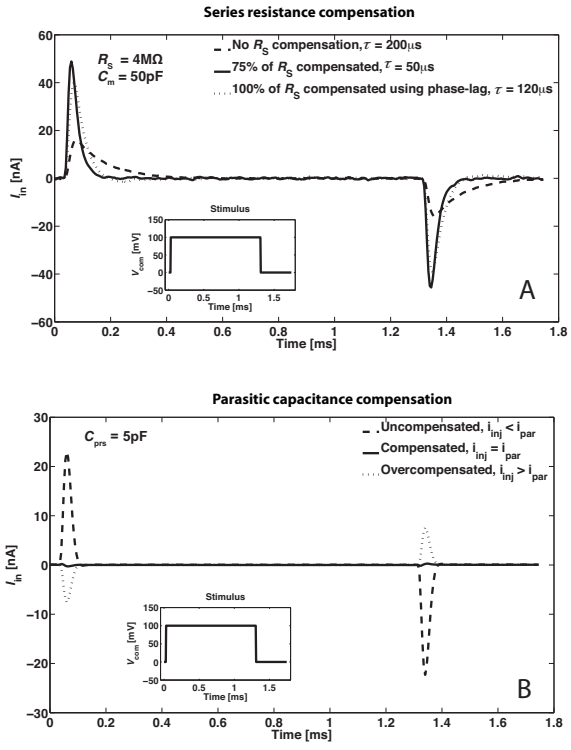

Fig. 3. Measured response of the electrode resistance (A) and capacitance (B) compensation circuits.

Fig. 5 shows measured simultaneous data from both channel of the system. In order to show the insignificant amount of cross-talk present in the multi-channel patch-clamp system,

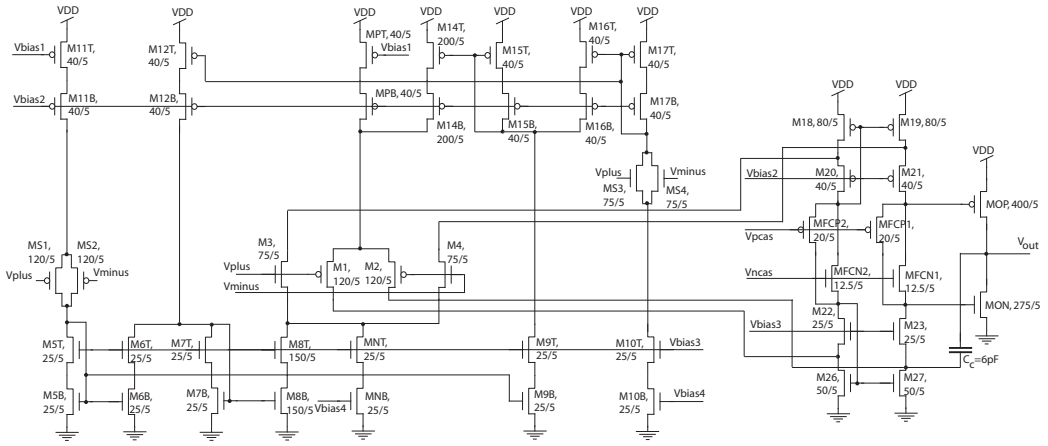

Fig. 2. Operational amplifier schematic.

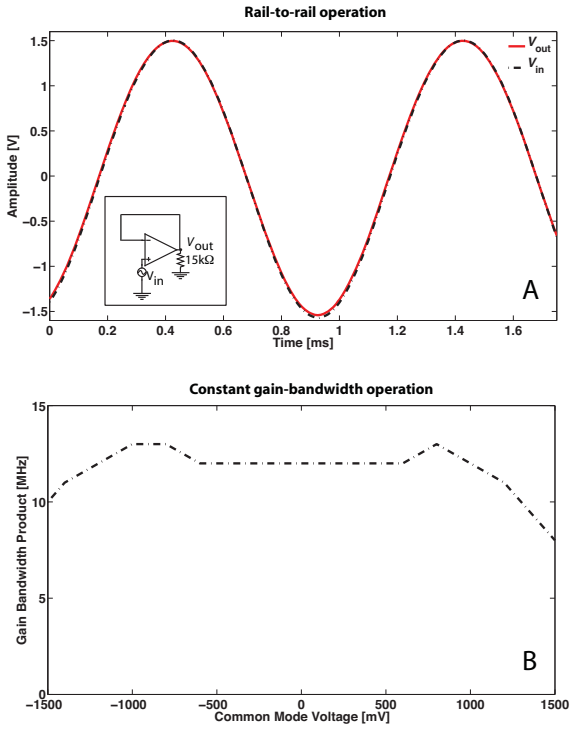

Fig. 4. Measured operational amplifier characteristics: (A) rail-to-rail operation, (B) constant gain-bandwidth over entire input common-mode range.

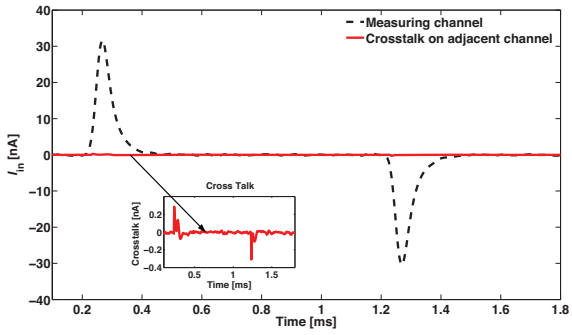

Fig. 5. Measured crosstalk between channels.

we have applied a large voltage step (100 mV) to one channel only. As can be seen in Fig. 4, the cross-talk on the adjacent non-measuring channel is -40dB in the worse-case scenario with 80% series resistance compensation applied.

Fig. 6-A shows inward currents recorded from Human Embryonic Kidney (HEK) 293 Cells expressing Na_v 1.7 sodium channels, one of the most demanding ion-channels to measure. The inset of Fig. 6 shows the protocol voltage steps applied to the cell membrane. A linear leak subtraction known as the -P/6 protocol was applied to remove leak currents [7]. This protocol (using six inverted pulse sequences scaled down by a factor of 6, delivered at negative membrane potentials) increases the net rms noise in the traces about three-fold. We compensated the 7 pF parasitic capacitance, and 80% of the 4.5 MΩ series resistance present at the input. R_f was set to 5 MΩ. Fig. 6-B reports the peak currents vs. V_{com} from Fig. 6-A. This smooth curve can only be obtained with a high percentage of R_S compensation and a highly linear patch-clamp system [7].

Table. I summarizes the key features of our patch-clamp recording system. Fig. 7 shows a die micrograph of the test circuit. The 2-channel system occupies 3 x 3 mm^2 of area and consumes 5 mW of power per channel. The input-referred noise is 8 pA rms at 10 kHz bandwidth. This result is comparable to state-of-the-art commercially available bench-top amplifiers. For example, the latest ionWorks amplifier from Molecular Devices has noise levels of 10 pA of rms current at 10 kHz bandwidth.

VI. Summary

We have implemented a two-channel patch-clamp system on silicon-on-sapphire in a 3 x 3 mm^2 area. There was less than -40 dB of cross talk between adjacent channels and the input-referred current noise of the system was 8 pA rms in a

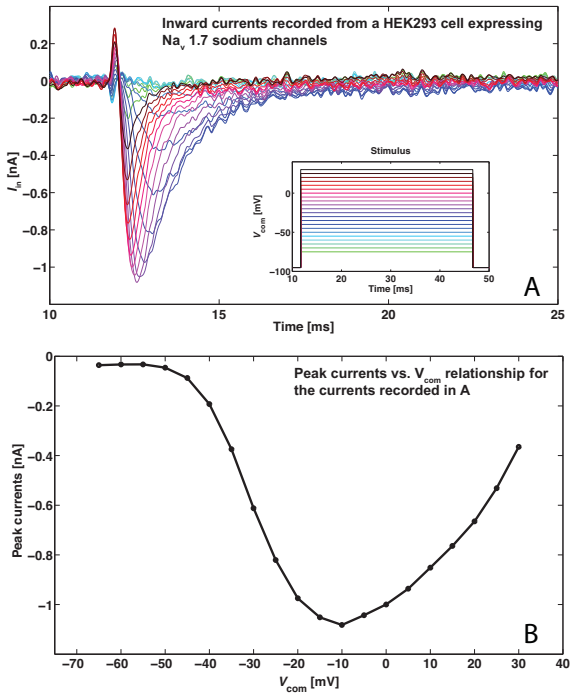

Fig. 6. Single-sweep responses of HEK 293 cells expressing Na$_v$ 1.7 sodium channels, after linear leak subtraction using the -P/6 protocol. The leak subtraction increases the net rms noise in the traces about three-fold. Rs was 4.5 M of which 80% was compensated. $C_{\rm prs}$ of 7 pF was fully compensated. Cm was 40 pF.

TABLE I
KEY FEATURES OF THE TWO-CHANNEL PATCH-CLAMP SYSTEM.

Technology	0.5 micron Silicon-on-sapphire
Number of channels	2 per die
Silicon area	3 x 3 mm^2 per die 1.5 x 3 mm^2 per channel
Power consumption	5 mW per channel at 3.3V
Capacitive compensation	10 pF max
Series resistive compensation	80 % of 100 MΩ or 100% with phase-lag compensation
Current noise	8 pA rms input-referred in a 10 kHz bandwidth
Variable feedback resistor	50, 100, 250, 500 kΩ 1, 2.5, 5, 10 MΩ
Dynamic range	± 20 μA
Reconstruction filter	2 poles, 80 kHz cutoff
Anti-aliasing filter	3 poles, 20 kHz cutoff
Linearity	$>$ 0.1 %
Cross talk between adjacent channels	-40 dB (at 80 % series resistance compensation)

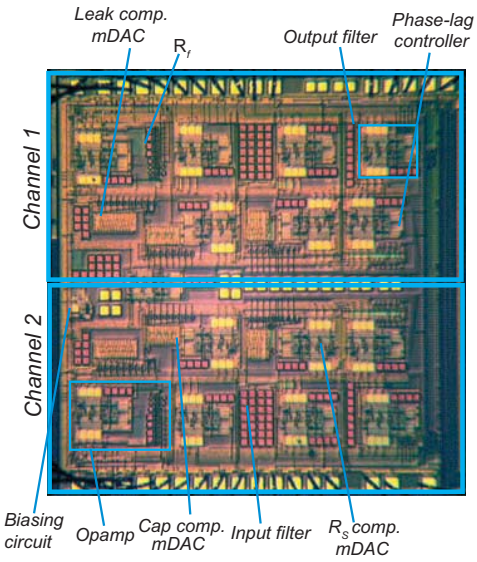

Fig. 7. A micrograph of the test circuit.

10 kHz bandwidth. The system is able to compensate series resistances and parasitic capacitances at the input The power consumption of the device was 5 mW per channel at 3.3 V. This accurate, low-noise system with electrode compensation can be used to produce massively parallel, high-throughput, patch-clamp systems.

VII. ACKNOWLEDGEMENTS

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