Monolithic digital galvanic isolation buffer fabricated in silicon on sapphire CMOS

E. Culurciello, P.O. Pouliquen, A.G. Andreou, K. Strohbehn and S. Jaskulek

A monolithic four-channel digital galvanic isolation buffer in the 0.5 μm silicon on sapphire (SOS) CMOS technology is reported. Advantage is taken of the insulating properties of the sapphire substrate to integrate on the same die both the isolation structure and the interface electronics. Each isolation channel has been tested to operate at data rates over 100 Mbit/s. The system can tolerate ground bounces of 1 V/μs and is tested for 800 V isolation. The system includes an integrated isolation charge pump to power the input circuit and is hence capable of operating from a single 3.3 V power supply.

Introduction: A digital galvanic isolation buffer is a device that communicates a digital signal from one physical region to another while preserving a galvanic isolation between the two regions. Galvanic isolation is desirable in locations with ground loops, or where it is not possible to ensure a common ground signal between output and input nodes such as biomedical equipment and instrumentation, control of high-voltage converters and circuits, and high voltage or high current industrial environments.

Conventionally, galvanic isolation buffers have been fabricated through the assembly of two separate dies packaged together as a hybrid structure, as in the case of optocouplers [1] and bulk capacitor based designs [2]. The cost of galvanic isolation buffers is high because existing solutions are not monolithic, necessitating expensive packaging procedures. Conventional bulk CMOS technologies cannot be used to design a monolithic isolation system on a single chip because the silicon substrate forms a galvanic connection between the input and output regions. A monolithic single chip digital isolation buffer has recently been reported using a silicon-on-insulator (SOI) substrate for interface circuits in data communication modem lines [3].

In this Letter we report on the design and fabrication of a monolithic single chip isolation buffer with integrated charge pump in silicon on sapphire CMOS technology for data communication and power transfer capable of 800 V continuous isolation with tolerance to ground bouncing of more than 1 V/μs.

System overview: The architecture of the system consists of a transmitter or input circuit, a receiver or output circuit, and a charge pump (Fig. 1). Differential signalling without modulation is used to drive two capacitors that block the DC signals between the input and output regions. Capacitive coupling of data has been employed in bulk CMOS multi-chip modules to transfer data between the die and the substrate in the multi-chip module [4–6].

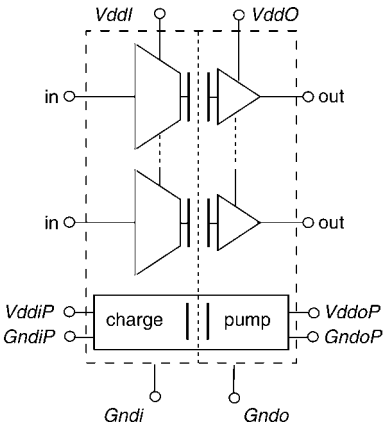

Fig. 1 *System architecture: four-channel isolation buffer*

A schematic diagram of one isolation channel is shown in Fig. 2. The input signal is buffered by digital inverters and communicated differentially to the output circuit using capacitive coupling. The coupling capacitors *C* have a value of 150 fF and have been designed as a parallel plate structure using the metal-1 and metal-3 layers. The coupling capacitance area is 175 × 60 μm^2. At the receiver side, low conductance current paths to power supply and ground nodes ensure that the voltage at the floating nodes always drifts towards one of the rail supplies.

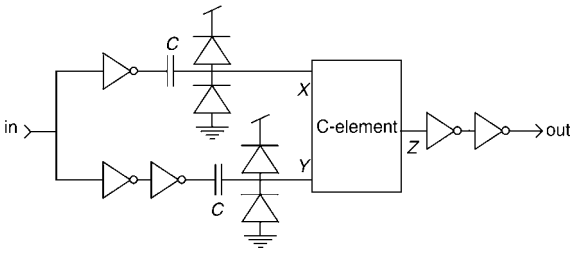

Fig. 2 *Capacitive isolator circuit: isolation cell*

A static asynchronous C-element [7], together with the dual rail signalling is employed to reject spurious transitions (Fig. 3). The C-element is a logic cell that switches its output only when it detects a valid differential transition. A valid transition is a transition where the inputs are of opposite signs. If only one of its inputs switches because of a ground bounce, the inputs will have the same polarity, and the output will not change.

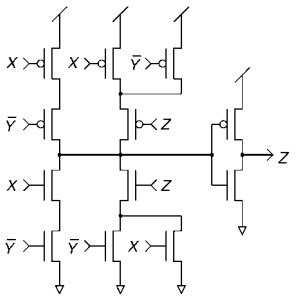

Fig. 3 *Asynchronous C-element circuit*

Fig. 4 shows a micrograph of the fabricated die. The final prototype of the capacitive isolation buffer is organised as an array of four independent isolation channels on a single chip. The output signals of the four channels are buffered with digital inverters to increase their drive capability to a 50 pF capacitive load at 100 MHz. All channels share the same input and output power supplies. The system can be powered from two separate supplies (*VddI* and *VddO* in Fig. 1): one for the input and one for the output. Alternatively, a single power supply can be used on the output side together (*VddO*) with an on chip charge pump to power the input circuits.

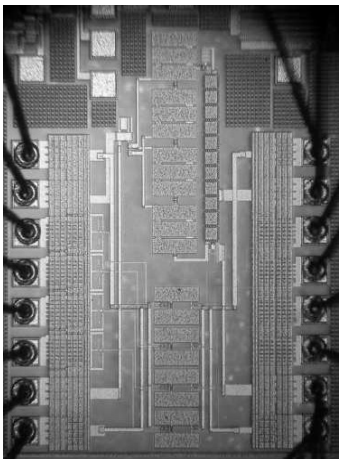

Fig. 4 *Die micrograph*

The on chip charge pump is based on the Dickson [8] architecture and it is driven by an 11-stage ring oscillator that provides a 350 MHz digital clock. The pump generates the required 3.3 V power supply with enough current (435 μA) to drive all four channels of the isolator at 100 MHz. The charge pump has separate external supply connections,

so it can be disabled to save power when both input and output side are externally powered.

Design, fabrication and testing: The circuits have been simulated at the design corners of temperature (−60°C, +130°C), transistor characteristics (typical, fast and slow), data rates (10 and 100 Mbit/s), two power configurations with and without the charge pump, and power supply variation (±10% of the nominal 3.3 V at 10 Mbit/s). In all cases the circuit was operational. All simulations have been conducted with all four inputs tied together, which corresponds to a worse case scenario for the charge pump loading.

The chips were fabricated through MOSIS (run T41H-T3CX). The total supply current for the four channels was 6 mA at 3.3 V, operating at 30 MHz with the charge pump off. No crosstalk from any channel to any other channel was observed. All measurements and results reported here were conducted with the isolation chip driving 2 ft of coaxial cable and a 25 pF load (oscilloscope load). Fig. 5 shows the output of one isolation channel (bottom trace) when driven with a 100 MHz input (top trace).

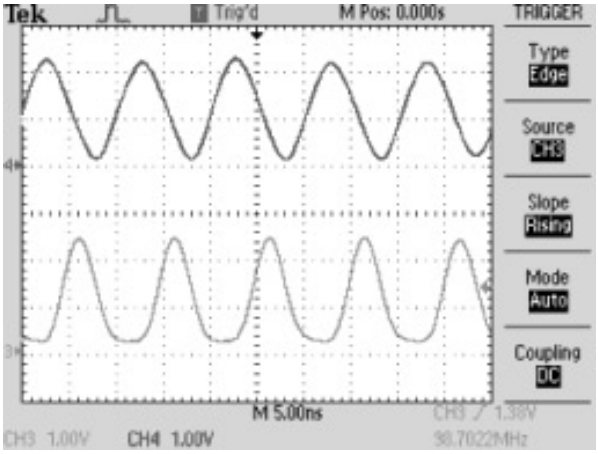

Fig. 5 *Measured experimental results*

When the charge pump was turned on, the static current consumption was 2.5 mA at a supply voltage of 3.3 V. The measured received power supply output of the charge pump was 2.68 V (unloaded). We measured the current drawn from the power supply for various operating speeds. At 1 MHz input square wave, the current was 3 mA, at 10 MHz it was 8 mA, at 30 MHz it was 10 mA. Driving all four channels in parallel with the same 30 MHz square input wave drew 14 mA. The current consumption of one channel at 100 MHz was 8 mA. The system, including the charge pump is capable of operation at a power supply as low as 1.5 V, with current consumption of 3 mA, at data rates of 30 MHz.

Isolation was verified experimentally, with the circuit operating with an input square wave of 30 MHz, at 3.3 V supply and ground signals for input and outputs set at a difference of 25 V. The limit for the isolation voltage was also measured separately and a breakdown of the structure was observed at about 800 V.

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