An Integrated Patch-Clamp Amplifier in Silicon-on-Sapphire CMOS

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***Abstract*—We designed and tested an integrated patch-clamp amplifier capable of recording from pico to tens of microamperes of current. The high-dynamic range of seven decades and the picoampere sensitivity of the instrument was targeted to whole-cell patch-clamp recordings. The prototype was fabricated on a 0.5-μm silicon-on-sapphire process. The device employs an integrating headstage with a pulse frequency modulated output, ranging from 3 Hz to 10 MHz. A digital interface produces a 16-bit output conversion of the input currents. We report on electronic characterization of the fabricated device, dynamic performance, and examples of measurements on biological cells for patch-clamp applications. The device will be used in an advanced planar high-throughput patch-clamp screening system for testing medicines.**

***Index Terms*—Biosensor, headstage, patch clamp, potentiostat, silicon-on-insulator (SOI), silicon-on-sapphire (SOS).**

I. Introduction

THE *patch clamp* is an extraordinary technique used in electrophysiology to measure the currents flowing through the membranes of living cells [1]. These recordings are crucial for the study of ion channels, which are the molecular structures responsible for membrane conductivity [2], [3]. All living cells that maintain a potential difference across their membranes contain ion channels serving as selective barriers, and channel dysfunction is associated with many common diseases such as diabetes and cystic-fibrosis. The patch clamp can measure the cell membrane conductance and is normally used to study the effect of drugs and medical treatments on ion channel dynamics. The progress of ion-channel research and the study of living cells is highly dependent on the availability of advanced instrumentation. Conventional patch clamp is a tedious and time-consuming process, requiring precise control of the testing equipment. There has recently been a great drive to develop systems which have high scalability and can operate with minimal manual control, and emerging technologies such as the planar patch clamp (shown in Fig. 1) are now beginning to make large-scale screens of genes and compounds possible [4]. The amplifier design described in this paper is the enabling technology, together with planar electrodes [5]–[8], necessary to realize the high-throughput system of Fig. 1. The targeted integrated system will be able to record from all the 96 well plates in parallel, as opposed to the 16 or 32 parallel recording available today only with bulky bench-top recording arrays [9], [10].

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Because of the importance of the patch-clamp technique in drug testing, pharmaceutical companies have long sought ways to increase the number of tests per unit time by using integrated circuits. The proposed instrumentation is now key to the development of pharmaceutical drugs. Recently, several common prescription medicines have been recalled or curtailed [11]. The peril is that these drugs can potentially contribute to patient's sudden death due to cardiac arrhythmias by prolonging the action potential in the heart's ventricles. As a result, the U.S. Federal Drug Administration now requires that every drug be screened for its impact on the length of ventricular action potential, and recommends a test for drug effects on ion-channel function [12]. The need for higher throughput screening instrumentation is thus a limiting factor for pharmaceutical companies' efforts to bring better and safer medicines to the consumer market.

In this paper, we present a high-performance integrated patch-clamp amplifier. Our design employs emergent integrated circuit technologies to provide low-noise amplification of ion-channel currents and high-density integration of electronic components. The silicon-on-sapphire (SOS) fabrication process for integrated circuits [13] features a non-conductive substrate, high-quality component isolation and multiple-threshold transistors. These features improve sampling speed and can significantly reduce electronic coupling noise in sensitive current-recording equipment such as patch-clamp amplifiers.

An integrated version of the patch-clamp amplifier not only reduces the size of the instrumentation, but also obtains better electrical performance, since cabling and parasitic capacitances that lower the measurement bandwidth are kept to a minimum. The implementation of the integrated circuit in SOS further reduces the capacitance by removing the influence of the substrate [14]–[16].

II. System Overview

Ion channel currents range from a few picoamperes for single-channel recordings to tens of nanoamperes for whole-cell measurements. Voltage steps between 10 and 100 mV are applied to the membrane during an experiment, in order to activate ion channel proteins and permit ionic currents to flow across the membrane. Currents are bi-directional, depending on channel type and membrane potential, and the bandwidth of interest is between a few hertz to 10 kHz in bench-top systems. Higher sampling rates and bandwidth are desired for more precise characterization of ion channels. The patch-clamp amplifier must have a large dynamic range in order to record the large transient currents after the stimuli, and must be highly sensitive to currents in the pico to nanoampere range. To this purpose, we have

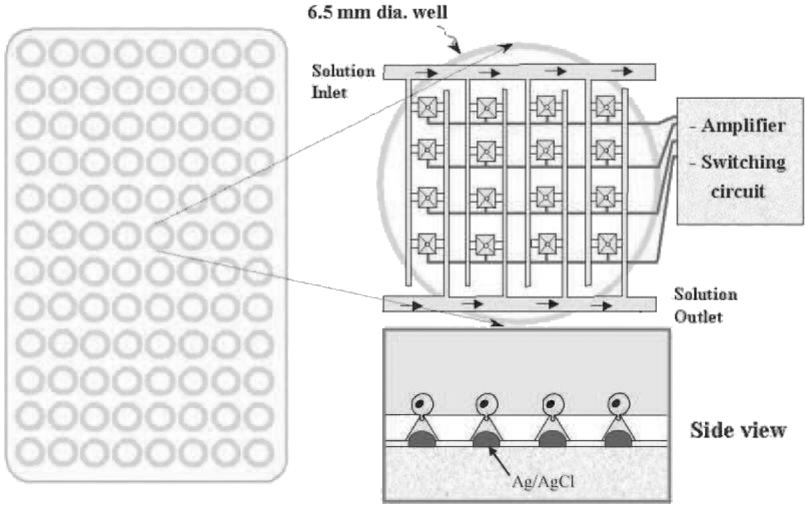

Fig. 1. Planar patch-clamp system. A suspension of cells is dropped on top of the planar electrode, and the geometry maximizes the probability of a cell sealing to the electrode. The integrated electronics presented in this paper enable densely packed array of electrodes systems for high-throughput patch-clamp measurements.

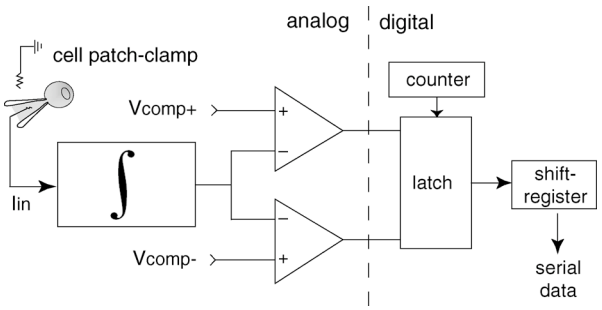

Fig. 2. Patch-clamp amplifier overview. The analog portion of the circuit integrates the input current up to a positive or negative threshold $V_{\mathrm{comp}+}$ and $V_{\mathrm{comp}-}$. After integration, a digital pulse latches an oversampled 16-bit counter to produce a digital output.

designed an integrated circuit based on asynchronous sigma-delta analog-to-digital converters [17]. The sensor is based on a pulsed-output current integrator circuit with reset frequency proportional to the input current [18]. This architecture permits high oversampling ratios at the bandwidths of interest. A block diagram of our patch-clamp system is shown in Fig. 2.

The input current is integrated over a capacitor until the integrator output reaches either of the compare voltages $V_{\mathrm{comp}+}$ or $V_{\mathrm{comp}-}$. At the end of integration, the change in the comparator's state generates a pulse. The digital components of the system comprise a 16-bit counter, latch, and shift register. The counter is free-running, and its value is latched when a pulse from the analog circuitry is detected. This value is then transferred to the shift registers, and serially communicated to a computer-based data-acquisition system. Since the output data is oversampled and synchronized by means of an external clock, the time between two integration pulses can be measured accurately. The difference between two latched values thus yields the integrator's reset frequency. This frequency can be used along with the system transfer function in (1) to calculate the input current

$$I_{\mathrm{in}} = C_f \Delta V f_{\mathrm{pulse}}. \tag{1}$$

I_{in} is the input current, C_{int} the integration capacitance used in the integrator, and ΔV is the voltage swing of the integrator.

The switched-capacitor headstage integrator was used in place of a conventional operational amplifier to reduce the noise reflecting on the headstage input capacitance. If an operational amplifier is used in the design, the input flicker noise level require the input transistor to be large. This in turn forms a large input capacitance where other noise sources from the clamp pipette would reflect and reduce the overall performance of the amplifier.

III. System Components

The patch-clamp technique is very sensitive to noise, due to the low amplitude of the membrane current [19]. In order to minimize the impact of the noise sources in our integrated system, we have employed a switched-capacitor implementation [18]. This realization also reduces the power consumption. There are two main components in the analog circuitry of our chip: the *integrator* and the *comparator*. All amplifiers are implemented using single-stage cascoded inverters which offer high-gain and low noise when operated in the subthreshold region [20]. The cascoded inverter schematic is shown as an insert in Figs. 3 and 4. The active transistor loads on the input transistor increase the gain of the inverter. The gain of the amplifier can be controlled by tuning V_{bias} and operating the circuit in the high-gain subthreshold region. From simulation, the cascoded inverter has a gain of 2000. The gain varies only 2% with a change of 10 K in temperature. This variation is not an issue in cellular experiments, where the temperature is kept constant by the measurement setup.

A. Headstage Integrator

A schematic of the headstage integrator is shown in Fig. 3. The integrator uses a user-selectable 60- or 600-fF feedback capacitor C_f to sense the input current. The integrator is initially reset to a reference voltage V_{ref}, chosen to be approximately at the middle of the integration voltage swing. Using

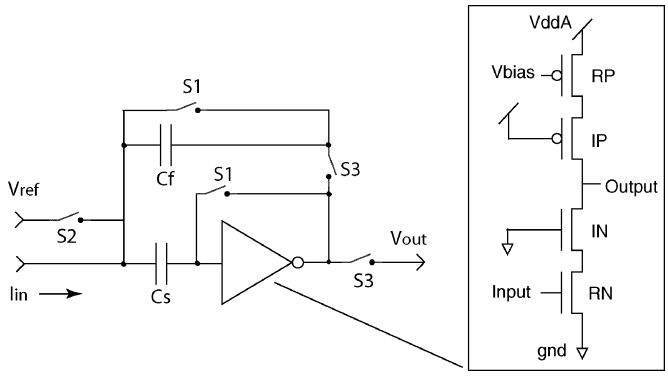

Fig. 3. Headstage of the patch-clamp amplifier is a current integrator. During the reset phase, switches S1 and S2 are closed. During the integration phase, switch S3 is closed. The cascoded inverter is portrayed in the insert.

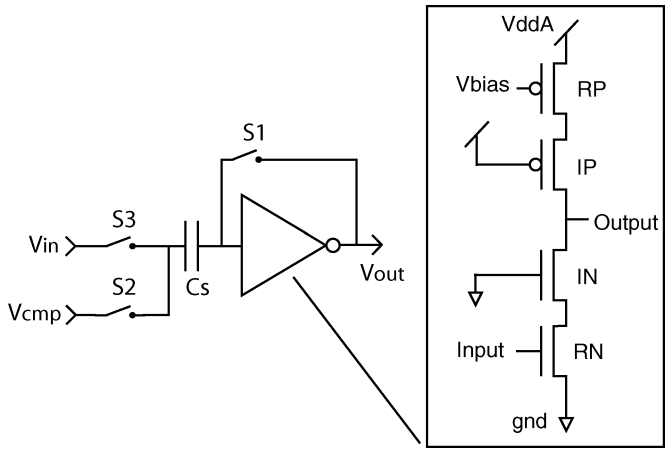

Fig. 4. Comparators used in the patch-clamp amplifier to detect the end of integration cycles. During the reset phase switches S1 and S2 are closed, while S3 is closed during the comparison phase. The cascoded inverter is portrayed in the insert.

a 3.3-V supply, $V_{\rm ref}$ is set to 1.6 V, to maximize the integration range. Since the system uses correlated double sampling (CDS), two samples are taken for each measurement. The first sample is taken during the reset phase of the system, when $V_{\rm ref}$ is connected to the input of the amplifier and switches S1 and S2 are closed. This voltage is stored on capacitor C_s of 1 pF, together with any correlated input noise. The input and output of the inverter are shorted, forcing both nodes to the inverter's logic threshold and highest gain. The second sample is collected during the operating phase of the circuit (switch S3 is closed), when the device is integrating the input current. Since the voltage noise is stored on C_s, the current seen by the integrator is the difference between the samples. Time-correlated noise such as flicker noise is thus partially subtracted from the integration voltage. The integrator's three-phase reset is designed to minimize the charge injection due to simultaneous switching. The switching sequence is S1, S2, and S3 in Fig. 3. We used compensated switches with dummy half-size transistors. We used transistors of the intrinsic kind for all the current sources, and to eliminate the need of biases in the cascode. The input transistor is of the RN kind to decrease the amplifier current and keep it in the subthreshold region. The transistor length and width was 2 μm.

B. Voltage Comparator

The comparator design uses the same principles as the integrator headstage. The schematic for the comparator is shown in Fig. 4. The input node is switched between the integrator output $V_{\rm in}$ and the compare voltage $V_{\rm cmp}$, and the amplifier is operating in open-loop configuration. The operation is divided in two phases. During the reset phase (switches S1 and S2 are closed), the compare voltage $V_{\rm cmp}$ is stored on capacitor C_s, together with any correlated noise. The inverter is also initialized to its logic threshold. During the comparison phase, switch S3 is closed. The input $V_{\rm in}$ is connected and the comparator changes state when this voltage exceeds $V_{\rm cmp}$. We employ two separate comparators in our circuit, one with a positive compare voltage and the other with a negative one with respect to $V_{\rm ref}$, as portrayed in Fig. 2. The value of $|V_{\rm ref} - V_{\rm cmp}|$ was set to 0.5 V to obtain a pulse frequency of approximately 10 kHz with an input current of 3 nA. The device logic circuitry is designed so that each comparator generates a positive output when it reaches the comparison point. This pulse latches the counter and serves as reset signal for the entire system.

IV. Input-Referred Noise Analysis

A. Patch-Clamp Noise theory

Noise in the patch-clamp amplifier can be categorized with respect to its place of origin into two main sources: the input transistor and the reset switches in the headstage integrator. The contributions of these sources are as follows.

- *The input transistor:* The input transistor of the headstage integrator is the major noise source in the patch-clamp circuit. The input transistor is the RN transistor in Fig. 3. The operating drain current though the transistor gives rise to shot noise. There are four transistors in the integrating headstage (including the input, as can be seen in Fig. 3), and each of these contributes to the total shot noise of the device. Moreover, the entrapment of electrons in the transistor gate oxide leads to flicker Noise, which varies as the inverse of the operating frequency. This noise source is the dominant noise source in the circuit at the low frequencies of operation of the patch-clamp amplifier (less than 10 kHz).
- *Reset switches:* The switched capacitor architecture of the patch-clamp amplifier introduces reset noise (kT/C noise) into the circuit as the capacitors are discharged through the finite resistance of the MOSFET switches. While adding a source of noise, this architecture enables the use of CDS and Flicker noise reduction and is thus ultimately beneficial to the overall design.

The total noise in the patch-clamp amplifier is the sum of the above-mentioned sources, and is given by

$$I_{\rm noise}^2 = I_{\rm shot}^2 + I_{\rm flicker}^2 + \frac{V_{\rm reset}^2}{Z_{\rm in}^2}[A^2]. \tag{2}$$

$Z_{\rm in}$ is the input impedance of the headstage. The major sources of noise and their contributions to total system noise at an operating frequency of 10 kHz are evaluated in Table I. The process parameters used for evaluation are given in Table II.

TABLE I
PATCH-CLAMP NOISE CONSTITUENTS EVALUATED AT 10 kHz

Type	I_n^2	value $[A^2]$	value $[A]$
Shot	$8I_dqf$	$3.84 \cdot 10^{-24}$	$1.95 \cdot 10^{-12}$
Flicker	$\frac{K_f g_m^2}{C_{OX} WLf^{A_f}} f(2\pi C_f)^2$	$1.37 \cdot 10^{-20}$	$1.17 \cdot 10^{-10}$
Reset	$\frac{kT}{C_{in}}(2\pi C_f)^2$	$5.84 \cdot 10^{-26}$	$2.41 \cdot 10^{-13}$

TABLE II
PROCESS PARAMETERS FOR NOISE CALCULATIONS

g_m	$4.51 \cdot 10^{-7} S$
C_{OX}	$2.47 \cdot 10^{-3} F/m^2$
A	$19.4 \cdot 10^{-12} m^2$
T	$298K$
I_d	$300 \cdot 10^{-12} A$
k	$1.38 \cdot 10^{-23}$
C_f	$60 \cdot 10^{-15} F$
C_{in}	$1 \cdot 10^{-12} F$
K_f	$1.28 \cdot 10^{-22}$
A_f	0.889

The total system noise is dominated by flicker noise at lower frequencies and by shot noise at high frequencies. Since the patch-clamp amplifier works in the kilohertz range, flicker noise would be the largest constituent of noise observed in these amplifiers. If the headstage was implemented as a regular operational amplifier, the only way to reduce flicker noise is to increase the size of the input transistor, at the expense of a significantly higher input capacitance.

B. Low-Noise Design for the Patch-Clamp Amplifier

In order to provide sensitivity in the picoampere range, we have employed an established technique to reduce flicker noise in our design. A noise correlated in time, flicker noise levels can be lowered using CDS [21]. This yields a lower noise system with the total input noise described

$$I_{\text{noise}}^2 = I_{\text{shot}}^2 + \frac{V_{\text{reset}}^2}{Z_{\text{in}}^2}[A^2]. \tag{3}$$

Once flicker noise is reduced, the total system current noise follows shot noise, which is at least one degree of order less than flicker noise (rms value) at the frequencies of interest. Fig. 5 shows a comparison between the total noise current expected in the patch-clamp amplifier with and without the use of CDS.

I, V are the elementary noise sources just described. Substituting the definitions of the noise sources into (3) yields

$$I_{\text{noise}}^2 = 8I_dqf + \left(4kTg_mf + \frac{kT}{C_{\text{in}}}\right)(2\pi f C_f)^2[A^2]. \tag{4}$$

In (4), I_d is the drain current through the input transistor, q is the charge of an electron, k is Boltzmann's constant, T is the ambient temperature, C_{in} is the CDS capacitor at the input node, and f is the frequency of operation.

Evaluating (4) at an operating frequency of 10 kHz, which corresponds to 3 nA of input current, yields 1.9 pA rms of noise current. The patch-clamp amplifier thus gives a high signal-to-noise ratio (SNR) in the nanoampere range. Notice also that integrating capacitance C_f must be much higher than the input capacitance of the headstage. Also the total noise is directly proportional to C_f, which should be minimized together with the headstage input capacitance. For this reason, a switched-capacitor headstage integrator design was used.

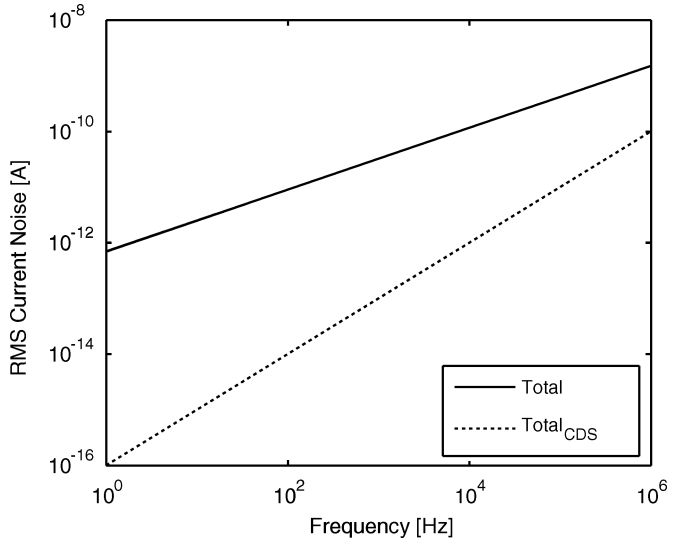

Fig. 5. Comparison between the computed total system noise with and without CDS. It can be seen that flicker noise subtraction by means of CDS is useful until gigahertz sampling frequencies.

V. RESULTS

We tested the integrated patch-clamp amplifier by sourcing a range of input currents from a few microamperes to a picoampere, while recording the frequency of the output pulse. The amplifier was powered at 3.3 V with an Agilent 3631A dc power supply. The voltage noise on the power supply and the bias voltages was measured as less than 2 mV rms. The input currents were sourced by applying a voltage across a megaohm resistor. A Keithley 2400 Source Meter was used to source and measure the input current. The frequency of the output pulse was measured using a Tektronic TDS2014 Four-Channel Digital Storage Oscilloscope. We obtained a linear transfer function across the entire range of tested currents in the range: [3 pA, 10 μA], as shown in Fig. 6. The output pulse frequency was in the range: [3 Hz, 10 MHz], and was observed to increase in discrete steps when very high currents were sourced as quantization noise due to low oversampling became dominant. We operated the device with clock frequencies of up to 50 MHz, and were thus able to extend the upper-limit of the current measurements. The use of fast clocks and the SOS process make this device one of the largest dynamic-range current measuring system reported [18].

The power consumption of the patch-clamp amplifier was estimated for both positive and negative currents and for both analog and digital supplies. The results for the nanoscale currents range of interest are plotted in Fig. 7. We observed that the power consumption increases at very low currents and low output pulse frequencies. The slow integration of low currents causes the digital interface to spend a long time near the logic threshold. This causes short circuit currents in the digital supply. Also notice the dependency of the analog power consumption on the direction of the current, due to charge injection. For higher

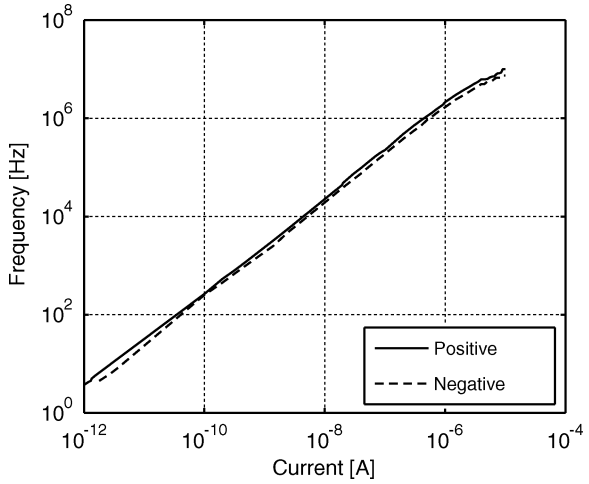

Fig. 6. Measured output pulse frequency of the headstage integrator as a function of positive and negative input currents, as integrated on a 600-fF capacitor. The dynamic range of the patch-clamp amplifier was measured to be 7 decades.

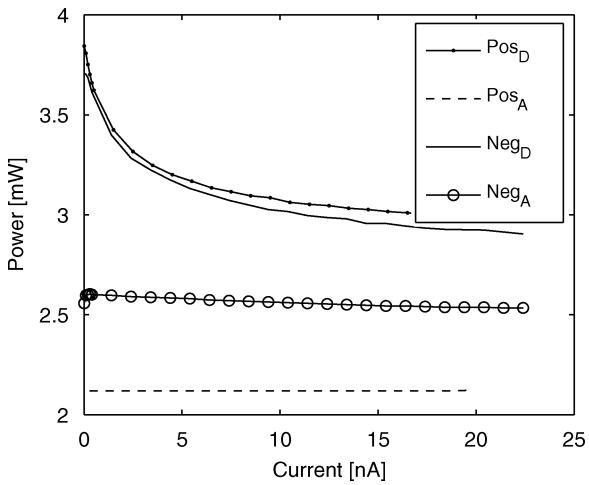

Fig. 7. Measured power consumption of analog and digital circuitry of the SOS integrated patch-patch amplifier. The power consumption was estimated for both positive and negative currents and for both analog and digital supplies.

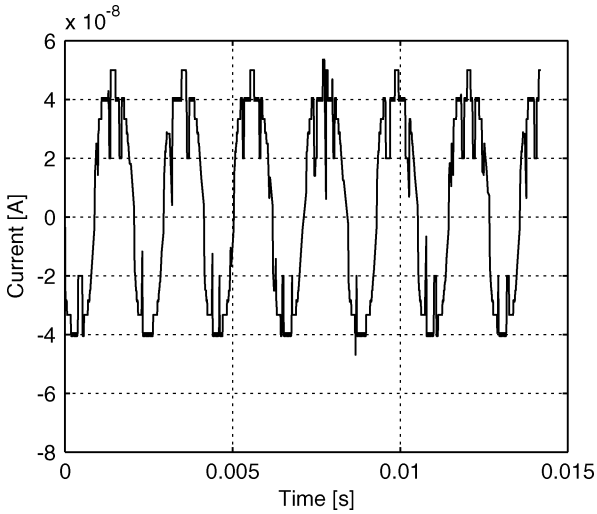

Fig. 8. Measured dynamic performance of the SOS integrated patch-patch amplifier. The input is a 400-Hz sine current of 50-nA amplitude sampled at 2 kHz.

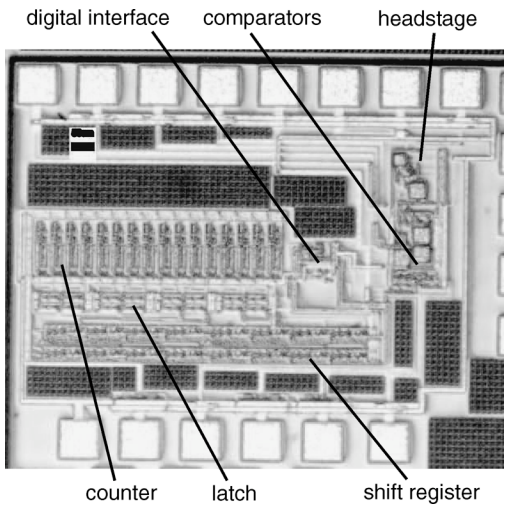

Fig. 9. Die micrograph of the SOS integrated patch–patch amplifier. The die size is 1260 by 1040 μm.

current (not in Fig. 7) both analog and digital power consumption increases with current as the reset frequency rises. The analog power consumption is mostly due to the short circuit current during the resent phase.

The dynamic performance of the patch-clamp amplifier was measured by digitizing a 400-Hz input sine current with an amplitude of 50 nA. The sampling rate was 2 kHz. Fig. 8 shows a plot of the recorded sine current and demonstrates the ability of our patch-clamp amplifier to record data at high-speeds. Notice that the glitches in Fig. 8 are due to readout errors of the patch-clamp amplifier data. We are working to eliminate this problem in the next version of the custom data acquisition software we are developing to operate the device.

The die size of the integrated patch-clamp amplifier measures 1260 by 1040 μm with pads and 1140 by 560 μm without pads. The headstage integrator measures 150 by 225 μm. A micrograph of the fabricated die is reported in Fig. 9.

VI. Experiments

To verify the usefulness of the patch-clamp amplifier in life-science applications, we used the patch-clamp amplifier to measure the ionic conductances of Rat Basophilic Leukaemia cells (RBL). Fig. 10 shows the gigaseal of a glass pipette to a RBL cell used in our measurements. The data collected from the RBL cells is due to inward rectifier potassium channels, which conduct only in the inward direction. The pipette solution used in the experiment was: 130 mM KCl, 10 mM NaCl, 1 MgCl2, 2 CaCl2, 10 HEPES, 1 EGTA, pH 7.4 with NaOH; the bath solution was: 130 mM KCl, 4.4 mM NaCl, 2 CaCl2, 2 MgCl2, 10 HEPES, 5 Dextrose, pH 7.4 with NaOH. Fig. 12 show the time response as step voltages are applied to RBL cells. The y axis shows the measured voltage (at the output of the analog filter), which relates linearly to the measured current.

A conventional patch-clamp experiment involves using a glass micropipette (with an aperture of 1 μm), and manoeuvering it to make contact and seal to the membrane of a cell residing in culture solution. The pipette contains the recording

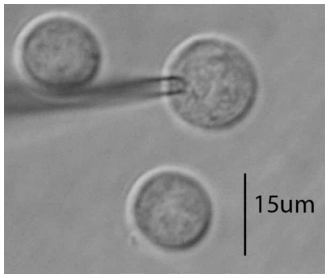

Fig. 10. Picture of the patch-clamp protocol on a RBL cell. A glass pipette is attached by gigaseal to one RBL cell of approximately 15 μm diameter.

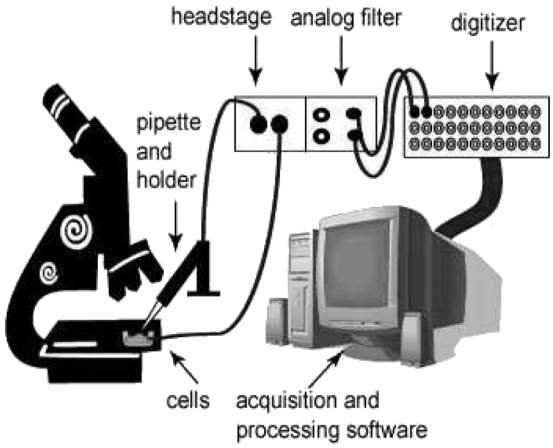

Fig. 11. Patch-clamp experimental setup.

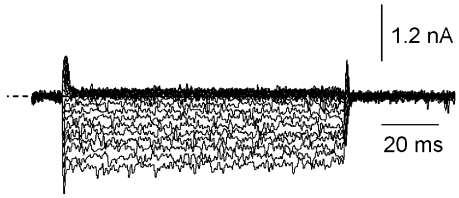

Fig. 12. Measured patch-clamp protocol on the RBL cells. The input current is converted to a voltage using the integrating headstage. The bath and pipette solutions both contained 130 mM of K+.

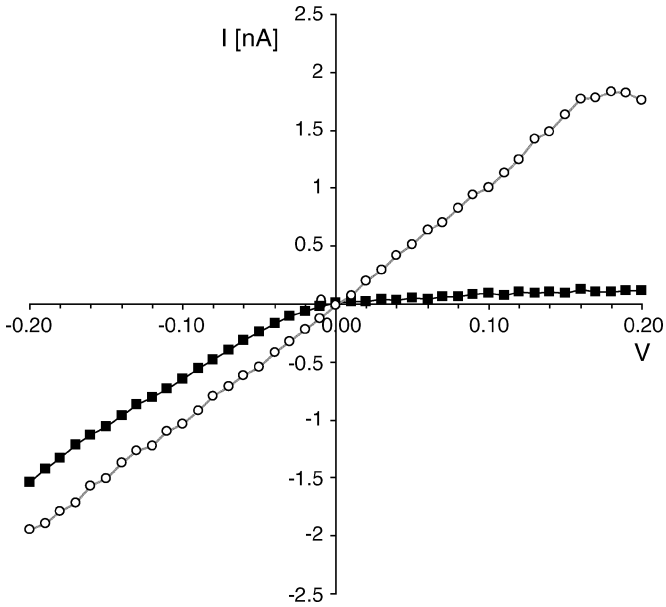

Fig. 13. Measured *I–V* characteristics on the RBL cells. This measurement is the mean current during the voltage steps. Notice the rectifying behavior of the RBL cells. The filled squares represent RBL cell current, and the open circles represent current through a 100-MΩ resistor.

electrode (also known as the patch electrode), and a command electrode is placed in the culture solution (known as the bath electrode). Suction is applied through the pipette in order to cause the cell membrane to rupture (wholecell configuration), thus shorting the electrode to the intracellular potential. Step voltages in the range of 10–120 mV are then applied between the patch and the bath electrode, and the corresponding ionic flow is measured. These voltage steps are applied to the $V_{\rm ref}$ terminal of Fig. 3. We have connected our device in series to a commercial patch-clamp amplifier, so that we could use its data acquisition software and real-time visualization. Digital-to-analog converters (DACs) driven by the commercial HEKA amplifier software were used to provide voltage steps to an external resistor connected to the amplifier's input node. We decoded the amplifier response by taking the digital reset pulse train at the output of the amplifier and *RC* filtering it with a time constant of 100 μm. The filtered positive and negative reset spikes were then passed through a difference amplifier and low-pass filtered using an analog 8-pole Bessel filter. This was equivalent to converting the variable-frequency reset spikes to scaled analog voltages and provided an efficient way for quantifying circuit current. The filter output was digitized at 10 kHz by standard patch-clamp software Digidata and visualized using Clampfit version 8.2. Our measurements were made using a standard patch-clamp setup, demonstrated in Fig. 11.

The inward rectifier measurements with the pipette clamped to the RBL cell are shown in Fig. 12. To obtain this figure, we applied step voltages from 200 mV down to -200 mV in 10-mV steps. With the pipette in the bath solution there is the equivalent of a 100-MΩ resistor between the electrodes. The analog filter 3-dB bandwidth was set to 500 Hz. The cell measurements are obtained by means of a gigaseal clamp implying that the seal resistance between the glass electrode and the cell membrane is larger than a gigaohm, and that current leaks are minimized. Notice that the ion channel is an inward rectifier potassium channel in the RBL cells, therefore it does not pass current in the positive direction. For this reason the *I–V* characteristic of the RBL cell measurement is one sided, as can be seen in Fig. 13.

The results of Fig. 12 obtained with our patch-clamp system are comparable in terms of noise performance to commercial automated systems [9], [10]. These are also designed for whole-cells recordings and have noise levels of 1–10 pA rms. Furthermore, the results of Fig. 12 are virtually identical to the recording with a commercial high-resolution patch-clamp amplifier as the Molecular Devices Axopatch 200B.

VII. Summary

We designed, fabricated and assembled an integrated patch-clamp amplifier targeted to whole-cell patch-clamp measurements. The device is capable of recording from pico to tens of microamperes of current, providing a very high-dynamic range and sensitivity. The prototype was fabricated on a conventional

0.5-μm SOS process, taking advantage of the low-power and low-noise property of the device and the insulating substrate. The device uses an integrating headstage with pulse-modulated output ranging from 3 Hz to 10 MHz and operating with a system clocks of 10 Hz to 50 MHz. A digital interface produces a 16-bit output conversion of the input currents. Finally, we have tested both the dynamic properties of the amplifier and have shown measurements on RBL cells typically used to characterized patch-clamp recording systems.

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