CMOS Low Current Measurement System for Biomedical Applications

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***Abstract*—We present a micro-chip implementation of a low current measurement system for biomedical applications using capacitive feedback that exhibits 190 fA of RMS noise in a 1 kHz bandwidth. The sampling rate is selectable up to 100 kHz. When measuring the amplifier noise with a 10 GΩ resistor and a 47 pF capacitor at the input, typical of cell membrane capacitance in DNA and patch clamp experiments, the measured RMS noise was 2.44 pA on a 50 pA signal in a 10 kHz bandwidth. Two channels were implemented on 630 × 440 μm^2 using a 0.5-μm 3-metal 2-poly CMOS process. Each channel consumes 1.5 mW of power from a 3.3 V supply. We measured the characteristics of an artificial lipid bilayer similar to the ones used in DNA sequencing experiments via nanopores.**

***Index Terms*—Amperometry, biomedical measurements, capacitive feedback, current measurement, integrator, low current measurement system, low noise circuit, noise analysis, potentiostat, voltage-clamp.**

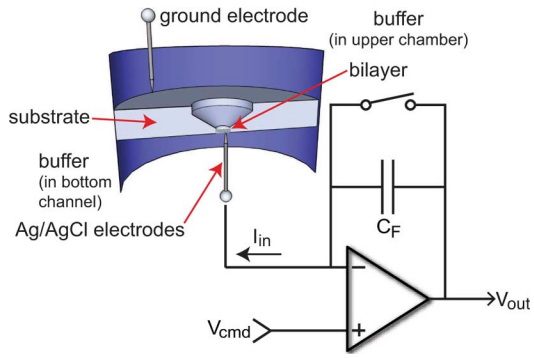

Fig. 1. Biomedical applications of this low current measurement system include bilayer patch measurements. A compact electronic headstage enables large bilayer measurement arrays.

I. Introduction

INTEGRATED multichannel low-noise current measurement systems are becoming extremely important components to interface and study physical phenomena at the sub-micro-scale for use in biological research and instrumentation. For example, patch-clamp is the electrophysiology gold standard technique to measure ion-channel currents when the cell membrane is "clamped" to commanded voltages. A low current measurement system (LCMS) is required to study the effect of drugs and medical treatments on ion channel dynamics [1], [2]. During single channel recording, the current level can be as low as tens of pico-amperes in 1–10 kHz bandwidth with a 50 pF electrode capacitance.

Another application that requires an integrated low current measurement system is a potential rapid DNA sequencing system where base pairs passing through a nanopore can be detected using current measurements in the range of 10–100 pA with a 10 kHz bandwidth and an input capacitance of 60 pF [3]. This system will dramatically reduce the cost and increase the speed of DNA sequencing and genomic research. Genomic information has a wide range of applications including human medicine, agriculture, security and defense, and evolutionary biology [4].

The use of artificial nanopores to monitor individual nanoparticles is a new technique that allows the use of nanoparticles as tags in biological assays, as substrates for multiplexed biological assays in solution, and as signal transducers in diagnostic assays [5]. This is another application where a LCMS is useful, in this case by clamping the voltage and measuring the current across the nanopore during the experiment.

A bilayer lipid membrane (or BLM) is an artificial membrane comprised of two mirror-opposed phospholipid sheets. When suspended across an aperture, the resulting bilayer membrane separates two aqueous compartments and mimics a native membrane without the other molecules which are normally present, including carbohydrates, cholesterol, proteins, and metallic ions [6]. Single-channel patch clamp can be considered a subset of BLM experiments. The use of the BLM in basic biological research has increased dramatically since its introduction and has been applied in numerous studies. The primary advantage of this system in these applications is the direct detection of single channel ion currents, unencumbered chemical and electrical access to both sides of the membrane for interrogation of modulators, the lack of a need for a living cell, and the ability to work with channel proteins that are not accessible by any other means (e.g., they reside within internal cell membranes). An example of a BLM experimental setup is shown in Fig. 1. Here, a small

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aperture in a substrate separates a well filled with a buffer solution into two chambers. A bilayer is suspended across the aperture. Electrodes are placed into the chambers and the LCMS, represented here by a schematic of an op-amp with capacitive feedback, is used to measure the properties of the membrane by clamping a desired voltage at one electrode with respect to the ground electrode and measuring the resulting current.

All of these measurements require a compact instrumentation headstage that has a very low input current noise at high sampling frequencies due to the magnitude and the speed of the signals being measured. It is very difficult to design a LCMS that can do high speeds such as 10 kHz with low-noise such as < 1 pA RMS input-referred noise measurements in the presence of a large load such as 60 pF because this input capacitance has a direct and large effect on the final measurement noise at such high frequencies. It is desirable to have an integrated system with a high dynamic range capable of being used in recording for all of these applications.

Commercial patch-clamp amplifier systems are available, such as Molecular Devices' Axopatch 200B [7] and the HEKA EPC-8 [8], but these systems are currently bulky, expensive, and not particularly suitable for simultaneous automatic measurements on a large number of cells in parallel, a very desirable feature for high-throughput essays and automated parallel systems [9]. A current amplifier front-end for nanobiosensors that uses a sophisticated integrator-differentiator circuit was presented in [10] and [11], but it requires a large silicon area which is less amenable to large array integration. Integrated systems have the advantage of reducing the electrode capacitance, which interacts with the voltage noise of the op-amp resulting in the main noise source of the system, and integrated systems can be used to realize multichannel systems to enable simultaneous and automatic measurement on a large number of cells in parallel. While an integrated patch-clamp system has been presented in [12], it is only for use in whole cell recording where the recorded currents are larger, in the range of 1–10 nA while typical recording bandwidths are 5–10 kHz.

While there is much literature on potentiostats, [13]–[15], many of these systems work in the nA or uA level or only achieve low noise when measuring at low frequencies, below the requirements of these applications. While some works do operate in the pA level [16], [17], or below, [18], they do not report low-noise levels at high sampling frequencies. For those that do report low-noise levels [19]–[21] these works do not report their noise at frequencies as high as 10 kHz. Additionally, many of the existing works use low or do not specify the input load capacitance used to achieve their results, or they measure internal current signals and do not show a real current measurement from off chip. We believe a thorough characterization must include the measurement noise in terms of the quantity being measured (or SNR), along with the bandwidth and load, as well as the typical measurement range, linearity, power consumption, and size. If different characterization is required for their application, it should be explained. An integrated system capable of measuring the pA range up to 4 kHz presented in [22] and [23] makes use of an oversampling ADC to reduce the measurement noise, but it provides no detailed theoretical model of its performance.

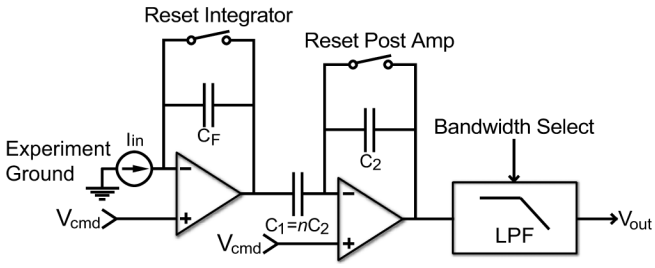

Fig. 2. System block diagram for the fabricated LCMS, featuring a current integrator for the first stage, followed by an inverting post amplifier stage. The operational transconductance amplifier (OTA) in the first stage performs voltage-clamping to the commanded voltage, $V_{\rm cmd}$, with respect to the experimental ground, and the input current is converted to an output voltage. The feedback capacitance of the integrator, C_F, is selectable as either 100 fF or 1 pF. The post amplifier can supply a voltage gain of C_1/C_2, or be bypassed based on the range of the measured input current. In our system $n = 10$, resulting in a gain of 10. The low-pass filter is used to filter out high frequency noise that is higher than the selected sampling frequency.

This work is the foundation for an integrated system capable of recording whole cell experiments and also single channel experiments. This work presents a low-noise integrated low current measurement system that features high bandwidth, sensitivity, and dynamic range to measure bidirectional currents in the range required for biomedical recording while allowing control of the voltage at the input node, known as voltage clamping and can be scaled up for use in an integrated multichannel system. We present a theoretical model for the measurement noise and our fabricated system shows good matching. Further, we demonstrate the system's usefulness by performing a measurement to characterize a lipid bilayer with results consistent with the literature.

II. System Overview

A. Architecture

The system, shown in Fig. 2, features a current integrator for the first stage with controllable gain, followed by an inverting post amplifier stage. The feedback capacitance of the integrator is selectable as either 100 fF or 1 pF and the post amplifier can supply a further gain of 10 or be bypassed based on the range of the measured input current. The low-pass filter is used to filter out high frequency noise that is higher than the selected sampling frequency. Finally, the signal passes through an output buffer that is capable of driving the output pad loaded by an external ADC. This system's basic design has been presented in [24].

In this system, an amplifier with capacitive feedback is used to fix the applied voltage to the cell under test. Either resistive or capacitive feedback could have been chosen, each with its own advantages and disadvantages. A resistive feedback system enables continuous time recording, while our capacitive feedback system is a discrete time system because it requires resetting the capacitor to avoid the amplifier reaching saturation. Capacitive feedback was chosen because a resistive feedback system would add thermal noise due to the resistor. In order to reduce the thermal noise of the resistor, a very large value resistor would

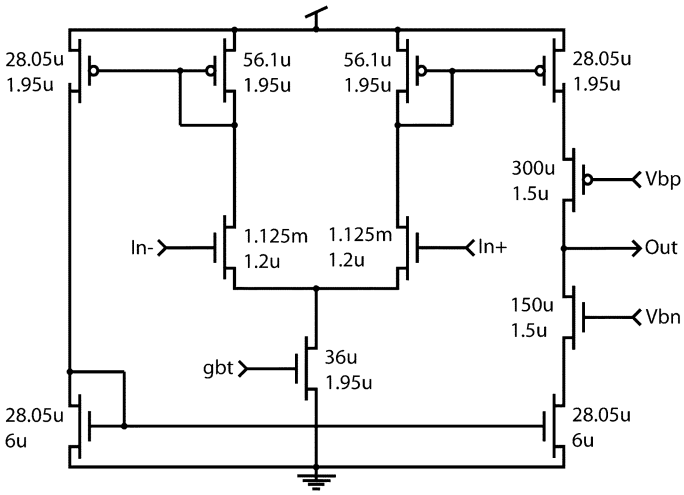

Fig. 3. Transistor schematic of the OTA used in the integrator. The specifications of the OTA are summarized in Table I.

TABLE I
SUMMARY OF THE DESIGNED OTA AND INTEGRATOR

V_{DD}	3.3 V
Bias Current	233 μA
Input Transistor Width	1.125 mm
Input Transistor Length	1.2 um
C_F	100 fF or 1pF
Open Loop DC Gain	90 dB
Phase Margin	60 degrees
Gain-Bandwidth Product with 60pF load	3 MHz
Minimum Reset Time	2 μs
Input Common Mode Range	1 V
Output Swing	1.5 V
Input-Referred Noise @ 10kHz	5.850 nV/$\sqrt{Hz}$
Input-Referred Noise @ 100kHz	4.715 nV/$\sqrt{Hz}$

be necessary which would have too much distributed capacitance when implemented in this 0.5-μm bulk CMOS technology [25]. The capacitive feedback system adds noise only due to the switching effect on the capacitor. The overall noise of the measurement with this system will depend on the equivalent input circuit and the sampling frequency, and has previously been analyzed in [26].

The current integrator consists of an OTA with a cascoded output stage and is shown in Fig. 3. The cascoded output stage boosts the gain of the mirrored OTA. Wide input transistors are used to reduce channel thermal noise, along with large area to decrease flicker noise. The input capacitance due to the transistors is much smaller than the electrode capacitance. In this technology, the NMOS mirror transistors exhibit higher levels of flicker noise than the PMOS, so the lengths of these were also increased. While a PMOS input pair could have been chosen for the lower flicker noise properties of PMOS transistors, their lower transconductance would have required more area and more power consumption to achieve the same overall noise level as choosing an NMOS input pair in this technology with this topology, so an NMOS input pair was chosen. The OTA tail transistor was biased for a current of 233 μA, while the current in the left and right branches is reduced by half, the ratio of the current mirror. This current was chosen to keep the overall power consumption reasonable for a mult-channel system while providing a high gain, low-noise, and enough driving current for the large capacitive load on the output. In open loop configuration, the DC gain is 90 dB which will ensure high linearity and reduce the clamping voltage offset between the channels. The integrator is periodically reset, so the OTA was designed to have a phase margin of 60 degrees when in a buffer configuration. The reset time of the integrator depends on the OTA bandwidth, which decreases with the load capacitance. With a high 60 pF load at the input from the electrode, which is also seen at the output during the reset, the GBP is 3 MHz and the minimum reset time is 2 μs. In this system, the integrator is the dominant noise source and was designed to have 5.850 nV/$\sqrt{\text{Hz}}$ of input-referred noise at 10 kHz and 4.715 nV/$\sqrt{\text{Hz}}$ at 100 kHz to compromise between power, noise, and area. The OTA has an output swing greater than 1.5 V. The common mode input range is 1 V, allowing for a wide range of command voltages to be applied. Typically only 100–500 mV are applied in patch-clamping. The integrator and its OTA were designed and simulated to have performance as summarized in Table I. The OTA was designed to achieve these specifications including its input referred noise, e_M, using the methods in [27] and [28].

The integrator has two phases: *reset* and *integration*. During the *reset* phase, the switch between the negative input terminal of the OTA and its output is closed, shorting the feedback capacitor and setting the output voltage to V_{cmd}. In this phase, the only noise source is the op-amp. During the *integration* phase, the switch is opened, the feedback capacitor has an initial charge of zero and integrates the input current. The resulting output voltage, V_{out} of this stage ideally is

$$V_{\text{out}} = \frac{1}{C_F}\int_0^{T_{\text{int}}} i(t)\,dt\,[\text{V}] \tag{1}$$

where C_F is the chosen integration capacitor, 100 fF or 1 pF, T_{int} is the integration time, and $i(t)$ is the input current to measure.

The op-amp offset and switching effects due to clock feed through and charge injection are eliminated off-chip by correlated double sampling (CDS). The CDS function reduces the effect of the low frequency noise by the subtraction operation. Since thermal noise is not correlated, the thermal noise is doubled, which is the reason for designing the OTA to exhibit low thermal noise.

Since the integration time is dictated by the sampling frequency, and C_F is limited by the manufacturing process limits, more gain may be required to sample the output voltage. The post amplifier can be enabled for this purpose. The inverting configuration is chosen to reduce the input common mode voltage range requirement. The gain of the post amplifier is determined by the ratio n, where $C_1 = nC_2$.

The low-pass filter is used to reduce the noise component above half of the sampling frequency and has a DC gain of 1.

The input current can be determined from the sensor's output voltage by first dividing by the voltage gain of each post amplifying stage, n, to determine the integrator's output voltage, and then converting this voltage to current by using the relation

$$I_{\text{in}} = \frac{C_F}{n}\cdot\frac{dV_{\text{out}}}{dt}\,[\text{A}]. \tag{2}$$

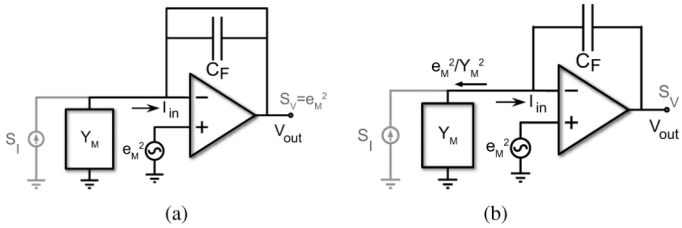

Fig. 4. Noise model for the capacitive feedback system during (a) the reset phase and (b) the integration phase. Here, Y_M is the admittance of the equivalent input circuit, and e_M is the input referred noise of the op-amp.

To perform the previously described CDS function digitally, two voltage samples are taken: one after the reset, V_i, and one at the end of the integration time, V_f. For a known time Δt between the two samples, the input current can easily be calculated as

$$I_{\text{in}} = \frac{C_F}{n} \cdot \frac{V_f - V_i}{\Delta t} \text{ [A]}. \tag{3}$$

B. Noise Analysis

The noise analysis of this capacitive feedback LCMS differs from that of a continuous time system because the integration time is not infinite. In order to analyze the noise performance of this system we need to separately calculate the noise for both operation phases. In multiple-stage amplification systems the noise contribution of the first stage is typically the dominant noise source of the system, therefore this analysis is for the integrator, but in reality the post-amplifier and filter add additional noise to the system.

During the *reset* phase, the feedback capacitor's terminals are shorted, configuring the op-amp as a voltage follower, as shown in Fig. 4. Thus, the only noise source is the op-amp. In this phase, the voltage power spectral density of the output equivalent voltage noise, $S_{V,\text{rst}}$ is calculated as

$$S_{V,\text{rst}} = e_M^2 \text{ [V}^2\text{/Hz]} \tag{4}$$

where e_M is the input referred noise of the op-amp. The equivalent input referred current noise, $S_{I,\text{rst}}$ in terms of the feedback capacitance and the integration time is

$$\begin{aligned} S_{I,\text{rst}} &= S_{V,\text{rst}} \cdot \left(\frac{C_F}{T_{\text{int}}}\right)^2 \\ &= e_M^2 \cdot \left(\frac{C_F}{T_{\text{int}}}\right)^2 \text{ [A}^2\text{/Hz]}. \end{aligned} \tag{5}$$

After reset, the feedback capacitor has an initial charge of zero. During the *integration* phase, the feedback capacitor integrates the input current, and the integrated output voltage during an integration time T_{int} can be represented by a convolution with the current and a rectangular time pulse, following from (1) as follows:

$$V_{\text{out}}(t) = \frac{1}{C_F} \cdot i(t) * (u(t) - u(t - T_{\text{int}})) \tag{6}$$

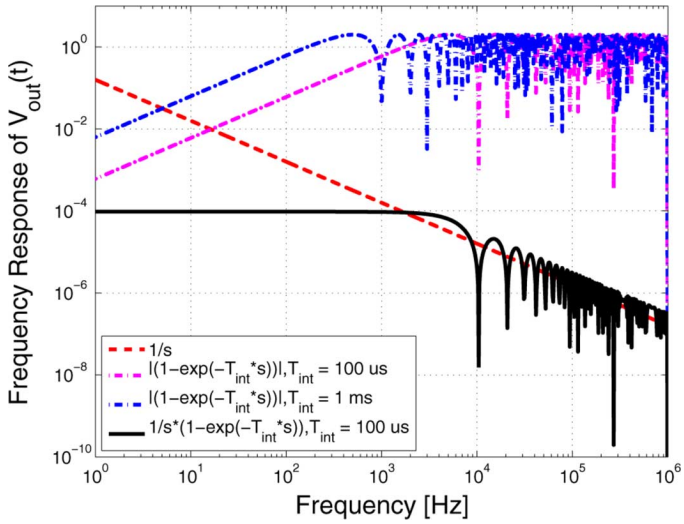

Fig. 5. Frequency response of the capacitive integrator $V_{\text{out}}(t)$ during an integration time, T_{int} (solid trace with $T_{\text{int}} = 100\,\mu$s). The response during the finite time is the combination of two terms: the current integration on the capacitor assuming infinite time (1/s) and the 1—exponential term, here presented with two values of T_{int}: 1 ms and 100 μs.

where $i(t)$ is an input current and $u(t)$ is the unit step function. Here, the Laplace transform of the expression in (6) can be obtained as

$$\begin{aligned} &\mathcal{L}\left(\frac{1}{C_F} \cdot i(t) * (u(t) - u(t - T_{\text{int}}))\right) \\ &\qquad = \frac{1}{C_F \cdot s} \cdot i(s) \cdot (1 - e^{-T_{\text{int}} \cdot s}) \end{aligned} \tag{7}$$

where $\mathcal{L}(i(t)) = i(s)$.

The frequency response of the capacitive integrator during an integration time T_{int} is shown in Fig. 5. The response during the finite time is the combination of two terms: the current integration on the capacitor assuming infinite time (1/s) and the 1—exponential term. The 1/s term and also the second term with two values of T_{int}: 1 ms and 100 μs are plotted. The final frequency response (solid trace with $T_{\text{int}} = 100\,\mu$s) is similar to a single-pole low-pass-filter.

From (7), the power spectral density of the output, S_V is calculated as

$$S_{V,\text{int}} = e_M^2 \cdot \left(\frac{Y_M}{C_F \cdot s} \cdot \left(1 - e^{-T_{\text{int}} \cdot s}\right)\right)^2 \text{ [V}^2\text{/Hz]} \tag{8}$$

where Y_M is the admittance of the equivalent input circuit. A model for the equivalent input circuit includes both the access series resistance of the electrode used to probe the unit under test along with its parasitic capacitance, as well as the resistance and capacitance of the actual unit under test.

From the above equations, the input referred current noise during integration $S_{I,\text{int}}$ is

$$\begin{aligned} S_{I,\text{int}} &= S_{V,\text{int}} \cdot \left(\frac{C_F}{T_{\text{int}}}\right)^2 \\ &= e_M^2 \cdot \left(\frac{Y_M}{T_{\text{int}} \cdot s} \cdot \left(1 - e^{-T_{\text{int}} \cdot s}\right)\right)^2 \text{ [A}^2\text{/Hz]}. \end{aligned} \tag{9}$$

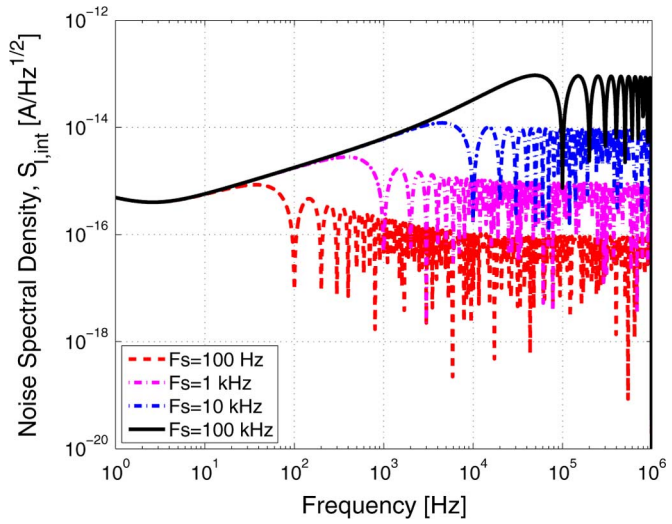

Fig. 6. Current noise spectral density of the integration phase for capacitive feedback system with different sampling frequencies F_S.

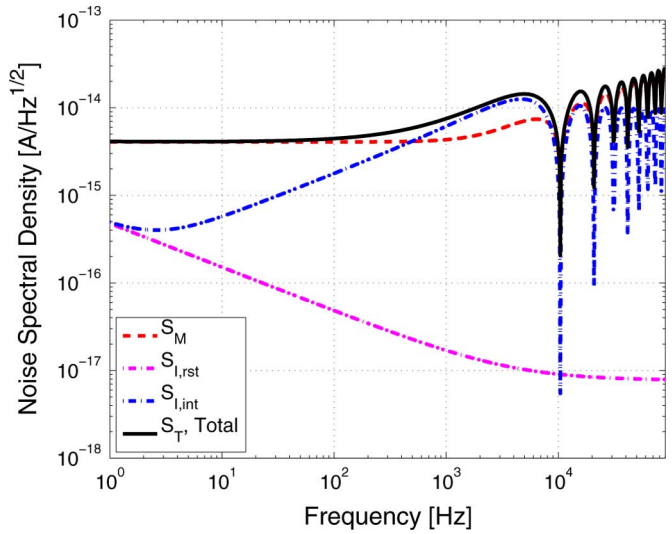

Fig. 7. Total current noise spectral density for capacitive feedback system with $T_{\text{int}} = 100\,\mu$s.

The input referred current noise during integration $S_{I,\text{int}}$ is plotted in Fig. 6 for a sampling frequency F_S of 100 Hz, 1 kHz, 10 kHz and 100 kHz, and clearly increases for higher sampling frequencies.

The total input referred noise, S_T, of the capacitive feedback measurement system is approximated as the sum of the noise current power spectral densities of the reset phase and the integration phase including the noise of the input equivalent circuit: $S_T = S_M + S_{I,\text{rst}} + S_{I,\text{int}}$, where S_M is the noise of the previously described input equivalent circuit [26]. Thermal noise is added from the real part of the input equivalent circuit, and the electrode capacitance and capacitance of the unit under test increase the admittance at higher frequencies. The noise components and the total noise are plotted in Fig. 7. Notice that at low frequencies the noise from the input equivalent circuit has a large affect while at higher frequencies the integration phase component $S_{I,\text{int}}$ is usually dominant.

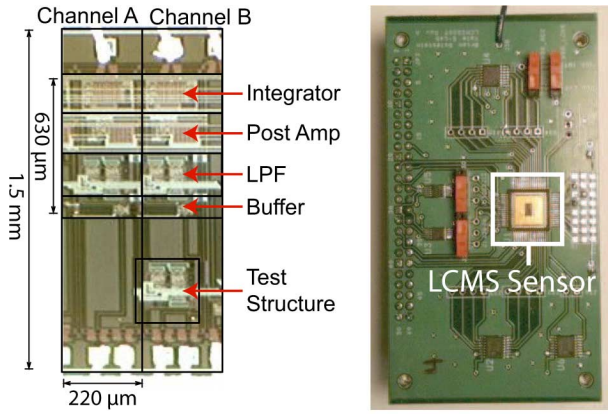

Fig. 8. (a) Die Micrograph: LCMS die micrograph, fabricated in the ON Semiconductor 0.5 μm 3-metal 2-poly CMOS process. Each channel is only $630 \times 220\ \mu\text{m}^2$. (b) System Board: The die installed in an LQPF package, shown with the lid removed, soldered onto a custom 4 layer PCB board with supporting circuitry.

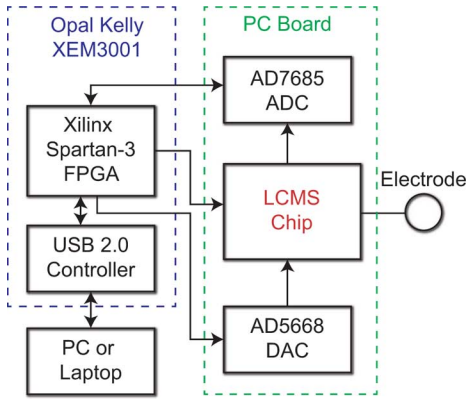

Fig. 9. Block diagram for the hardware testbed, which consists of the LCMS sensor, an AD7685 ADC, an AD5668 DAC, and an Opal Kelly XEM3001v2 board featuring a XIlinx Spartan-3 FPGA and USB Controller to communicate with a PC for user configuration and data logging.

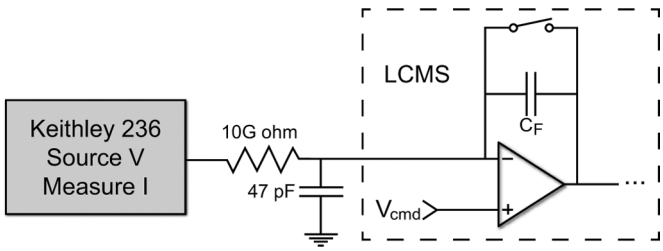

Fig. 10. The LCMS was tested by applying voltages across a 10 GΩ resistor using a Keithley 236 Source Measure Unit to generate a known current. Load capacitors up to 47 pF were inserted to simulate electrode load capacitance.

III. Measurement Results

A. Hardware Test Bed

The designed LCMS was fabricated in a 0.5 μm 3-metal 2-poly CMOS process, which has the advantage of being inexpensive, and the die micrograph is shown in Fig. 8(a). We designed a custom 4-layer printed circuit board (PCB) with separate analog and digital power planes to minimize the noise on the PCB level shown in Fig. 8(b). The fabricated LCMS has

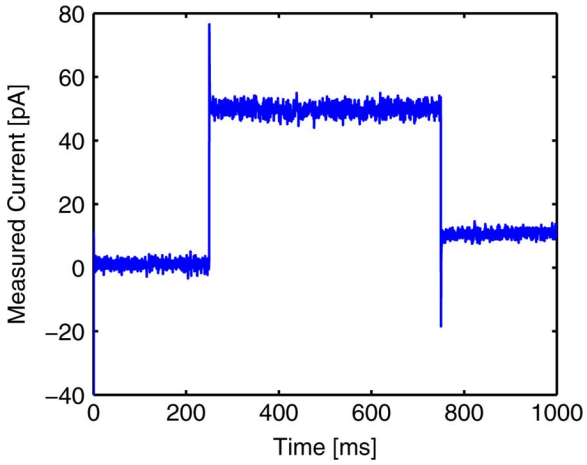

Fig. 11. Measured current output of a 50 pA followed by a 10 pA stimulus using a 10 GΩ resistor, showing 1.35 pA RMS noise at a sampling rate of 10 kHz when $C_F = 100$ fF.

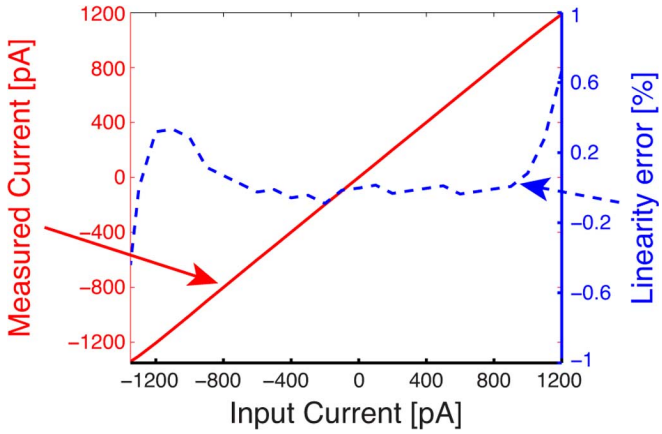

Fig. 12. Linearity Error Measurement Results for $C_F = 100$ fF, taken at a 10 kHz sampling rate by sweeping the command voltage and measuring the input current. The measured value was then compared with the expected value and the measured percentage difference is reported.

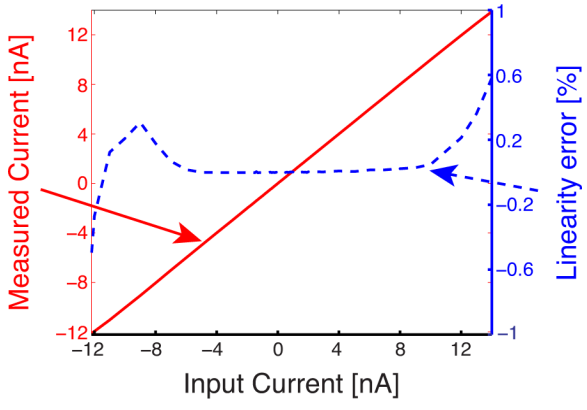

Fig. 13. Linearity Error Measurement Results for $C_F = 1$ pF, taken at a 10 kHz sampling rate by sweeping the command voltage and measuring the input current. The measured value was then compared with the expected value and the measured percentage difference is reported.

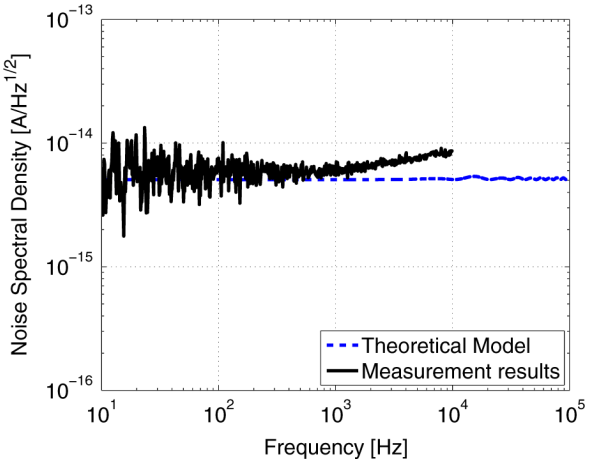

Fig. 14. Measured Noise Spectral Density when $C_F = 100$ fF. The theoretical model includes the integrator noise, the shot noise of the leakage current at the input, and the noise of the output buffer which drives the ADC.

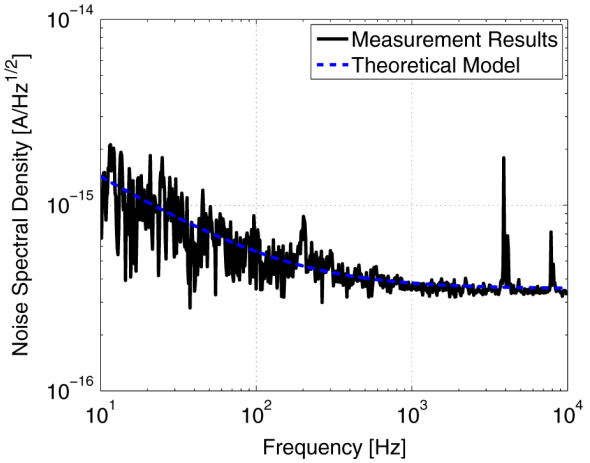

Fig. 15. Measured Noise Spectral Density during reset phase. The theoretical model for the integrator is shown along with a model which includes the integrator reset noise, the shot noise of the leakage current at the input, and the noise of the output buffer which drives the ADC.

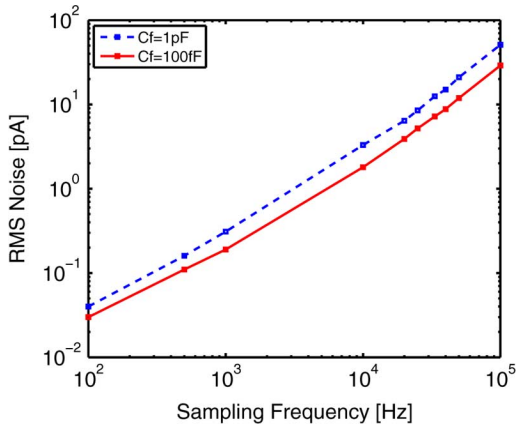

Fig. 16. Measured RMS Current Noise for both $C_F = 100$ fF and $C_F = 1$ pF at different sampling frequencies.

two channels, each occupying 630×220 μm^2 die area. The external ADC, an Analog Devices AD7685, features 16 bits of resolution and 250 kSPS. The external DAC for supplying bias voltages and V_{cmd} was an AD5668. The system uses an Opal Kelly XEM3001v2 board which features a Xilinx Spartan-3 FPGA and a USB Controller to communicate with a PC for

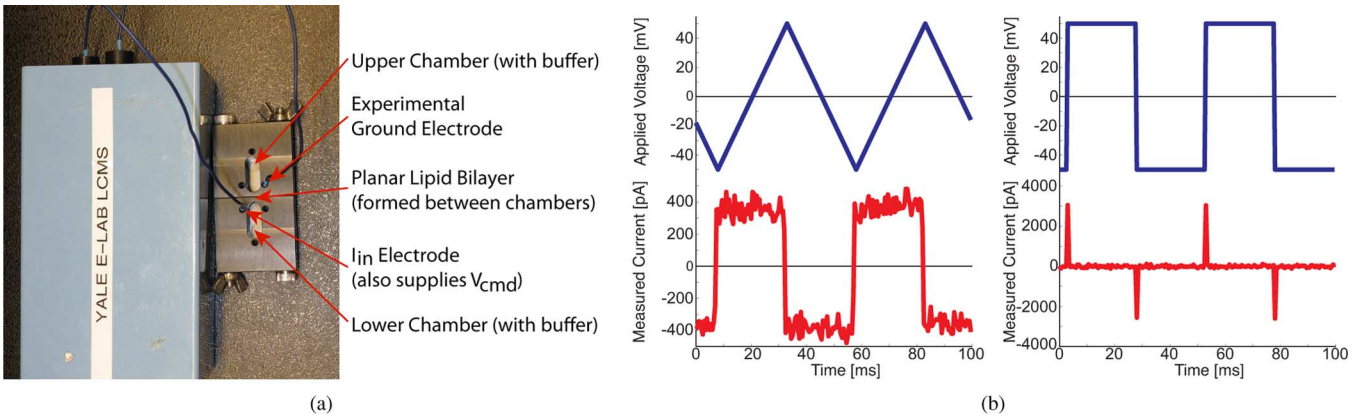

Fig. 17. Experimental setup using our LCMS to measure the current across a black lipid membrane in a hole of Teflon film. (a) The experimental setup. (b) The applied signal and measured current. From the recorded signals, the specific capacitance of the lipid bilayer was calculated as 1.0495 μF/cm^2 and the specific resistance as 1.7365 MΩcm^2, which is consistent with the reported properties of the black lipid membrane [29].

user configuration and data logging. The hardware testbed is shown as a block diagram in Fig. 9.

B. Hardware Characterization

The LCMS was tested by applying voltages across a 10 GΩ resistor using a Keithley 236 Source Measure Unit to generate a known current, as shown in Fig. 10. Generating a known small current with low-noise is best done by applying a voltage across a large resistor in this fashion. Load capacitors up to 47 pF were inserted to simulate electrode load capacitance, which greatly affects the overall noise performance. A 500 mV stimulus was applied after 250 ms followed by a 100 mV stimulus at 750 ms, resulting in a 50 pA current followed by a 10 pA current which were accurately measured by the LCMS with 1.35 pA RMS input referred noise at a 10 kHz sampling rate as shown in Fig. 11. After adding a 47 pF capacitor at the input, typical for the intended applications, the measured RMS noise was 2.44 pA at the same sampling rate. The linearity error with a 100 fF and 1 pF integrating capacitor was measured and is less than $\pm 0.5\%$ for the input current range of (-1300 pA 1200 pA) @100 fF, (-12 nA 13 nA) @1 pF and is presented in Figs. 12 and 13. By switching between the available on-chip integrating capacitors, the measured dynamic range is 83 dB with less than $\pm 0.5\%$ linearity error at a 10 kHz sampling rate. If the integrating capacitor is not switched, a dynamic range of 63 dB was measured at the same sampling rate. The noise spectral density was recorded with $C_F = 100$ fF by disconnecting the input and tying the command voltage to the experimental ground, and is shown in Fig. 14 along with theoretical model. The measured performance matches the theoretical model here, which is the same as in Section II.B with the addition of noise due to the shot noise of the leakage current at the input, and the noise of the output buffer which drives the ADC. For completeness, the noise spectral density during the reset phase was also measured in the same fashion but this time with the reset transistor on, and is shown in Fig. 15 along with the model. Again, the measured performance matches the model. We believe the spikes at 4 and 8 kHz are due to aliasing and would normally be removed by the low pass filter, however the filter is not used in this measurement since we are focusing on comparing the measured noise of the integrator to our model. The measured RMS current noise was recorded using the same technique for both $C_F = 100$ fF and $C_F = 1$ pF at different sampling frequencies and is presented in Fig. 16. The noise increases with the sampling frequency, as the model predicted.

C. Measuring the Electrophysiological Properties of a Planar Lipid Bilayer

The LCMS was then used to characterize the electrophysiological properties of a planar lipid bilayer. A planar lipid bilayer was formed in a hole of Teflon membrane between two aqueous compartments. The apparatus for forming the bilayer allows electrode access to the compartments allowing us to measure the bilayer using our LCMS as shown in Fig. 17(a) and was created as described in [30]. The lipid bilayer was then created by the Montal-Mueller method [31]. In order to characterize the bilayer, square and triangular stimulus voltage signals, shown in the top of Fig. 17(b), from an external function generator, were applied while the resulting currents through the lipid bilayer were recorded by the chip shown in the bottom of Fig. 17(b), below their corresponding stimulus. The bilayer can be modeled electrically as an RC parallel circuit. From the recorded signals, the specific capacitance of the lipid bilayer was calculated as 1.0495 μF/cm^2 and the specific resistance as 1.7365 MΩcm^2, which is consistent with the reported properties of the black lipid membrane [29]. While the Keithley tests indicate our sensor should have less noise than we recorded during this experiment, we also measured the noise when the electrodes were placed in a 1M KCL solution (the same solution the bilayer was created in) where we measured an RMS noise of 26 pA. When performing the same test with a commercial amplifier at the same sampling rate, the Axopatch 200B with a 10 kHz LPF, we observed an RMS noise of 33 pA.

IV. Conclusion

In this paper we have demonstrated that amplifiers using capacitive feedback are capable and useful for integration in voltage-clamping low current measurement systems. We have presented an OTA current integrator based LCMS and its theoretical noise model which shows good matching with

our fabricated system. We have measured the performance of the system and demonstrated its usefulness in biomedical applications by using it to characterize a lipid bilayer. The measurement noise depends on the noise of the equivalent input circuit, the noise of the op-amp, the size of the integration capacitor, and the integration time. We believe capacitive feedback to be capable of very low levels of noise and to have superior noise performance compared to resistive feedback systems that are usually dominated by the thermal of noise of their feedback resistor.

Because high frequency noise is the dominant component of the overall RMS current noise, especially when high sampling frequencies are desired, we recommend using an amplifier with very low thermal noise levels. The amplifier must also have enough common mode range to cover the clamping voltage range, enough output swing to avoid saturation within the integration time for the given integration capacitor and input current, and high linearity, such as in the system presented in this work. CDS can be used to reduce flicker noise. Because any noise on the command voltage adds to the clamping voltage and therefore output noise, we recommend having a very clean command voltage or add an input low pass filter on the chip to filter out noise on the stimulus. Because the input equivalent circuit also contributes noise, especially at lower frequencies, we advise users to minimize parasitic input capacitance. Additionally, leakage current can contribute shot noise to the input and should be minimized. We also advise users to minimize external environmental noise sources by working in a faraday cage.

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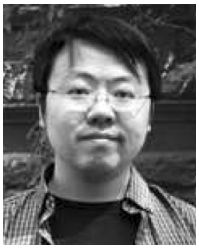

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