An Integrated Patch-Clamp Potentiostat with Electrode Compensation

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***Abstract*— We present the first fully-integrated implementation of a patch-clamp measurement system with series access resistance and parasitic capacitive compensation capability. The system was implemented in a 0.5μm silicon-on-sapphire process and is capable of recording cell membrane currents up to $\pm$20nA, with a rms noise of 5pA at 10kHz bandwidth. The system can compensate for the capacitance and resistance of the electrode, up to 20pF and upto 70% of the series access resistance respectively. The die size is 1150 by 700μm. The power consumption is 300μW at 3.3V. The integrated patch-clamp system will be used to fabricate high-throughput planar patch-clamp systems.**

I. Introduction

The patch-clamp is the gold standard in electrophysiology and is a fundamental technique to screen drugs and medical compounds, and ultimately to ensure consumer safety [1], [2]. Electrophysiologists use the patch-clamp technique to measure the currents flowing through the membranes of living cells. The currents measured by the patch-clamp is used to study the effect of medical compounds and the behavior of ion channels, the structures responsible for cell membrane conductivity [3]. The patch-clamp technique reports the highest signal-to-noise ratios available in a biosensor, but is labor-intensive when performed manually. In whole-cell patch-clamp recording, the ion-channel current across the whole cell membrane is measured while clamping the membrane at a known potential. Two whole-cell recording setups are shown in Fig. 1. In conventional patch-recordings, a glass pipette is used as the electrode. The pipette is filled with ionic solution and is attached to the cell using micro manipulators under a microscope. Suction is first applied so that a tight seal ($\sim 10^{10}\Omega$) is formed between the pipette tip and the cell membrane. Further suction is applied to break the cell membrane and gain access to the interior of the cell. The second electrode is placed on the bath solution in which the cell is immersed. A planar patch-clamp setup is shown in Fig. 1 (B). In planar whole-cell patch-clamping, the cells are suspended on top of a micro pore on a plane surface. A seal and access to the interior to the cell is established by applying suction. Since no micro-manipulation is necessary, this process can be automated.

In this paper, we present a silicon-on-sapphire integrated patch-clamp measurement system, an enabling technology when used with planar electrodes [4]–[8], to perform simultaneous and automatic measurements on a large number of cells

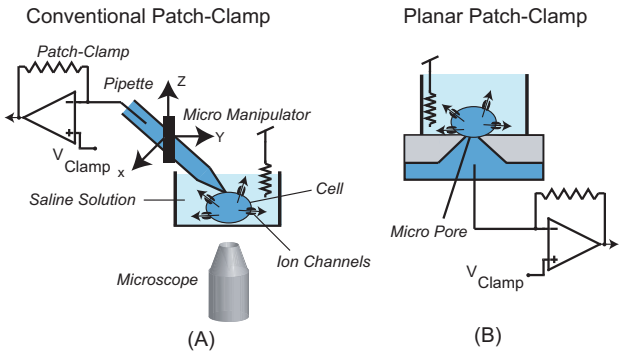

Fig. 1. A. In conventional whole-cell patch-clamp recordings, a pipette filled with electrolyte solution is used as the electrode. It takes considerable skill to attach the pipette to the cell using micro-manipulators and a microscope. B. In planar patch-clamp technology, cells are adhered to an aperture using suction. No micromanipulation is necessary.

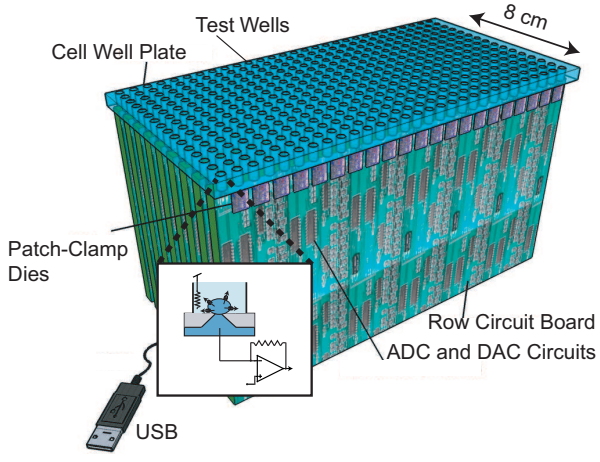

Fig. 2. A high-throughput patch-clamp system comprised of integrated patch-clamp amplifiers and planar electrodes. This system allows to perform simultaneous patch-clamp recordings on an entire 384 well plate.

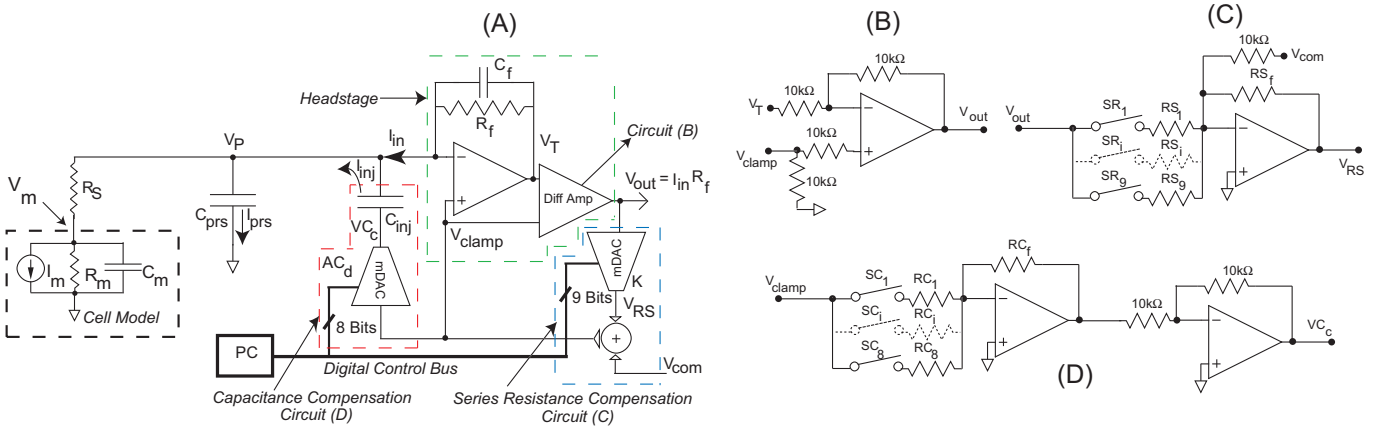

Fig. 3. (A) Block diagram of the integrated patch-clamp recording system with electrode compensation. A trans-impedance amplifier followed by a difference amplifier produces an output proportional to the input current. Two compensation circuits provide electrode capacitance and resistance compensation. The amount of compensation is controlled by two multiplying digital to analog converters (mDACs). The device was designed to measure cell membrane currents of ±20nA. (B),(C),(D) shows the difference amplifier, series resistance mDAC and capacitive compensation mDAC implementation in (A).

in parallel. Since the diameter of a standard cell well is only a few millimeters, a high-density patch-clamp system such as the one in shown in Fig. 2 can be realized only if the patch-clamp circuitry can also be miniaturized to millimeter sized dimensions [9]. An amplifier can be placed beneath each test well to facilitate recording from multiple cells. The output of the cell plate can be later multiplexed into a serial data stream to be transported to computer for processing. Our design is a fully integrated patch-clamp and is 10 million times smaller in volume than commercial bench-top systems. Other than minimizing the space requirements, an integrated patch-clamp amplifier reduces noise and offers better electrical performance by decreasing cabling and other parasitic capacitances that lower the measurement bandwidth. Although integrated circuits able to measure whole-cell currents have been previously realized, they lack the essential ability to compensate for the resistance and the parasitic capacitance of the electrode [7], [10]–[14]. In whole cell recordings, the entire cell membrane contributes to the charging time constant. The series resistance of the electrode is typically 5-20MΩ and the cell membrane capacitance is typically about 12pF or more leading to access time constants (τ_a) of in the order of milliseconds. This access time constant is also the time constant for the membrane current (I_m) to reach the current measuring circuitry [15]. Electrophysiologists are interested in recording ion-channel activity with a resolution of about 150μs. Therefore, compensation circuitry to increase bandwidth is an indispensable component of a whole-cell patch-clamp system. In our design, we use a large resistor in conjunction with an operational amplifier to obtain linear amplification of current. By using SOS technology, we have minimized the significant parasitic capacitance of resistors made in conventional bulk CMOS processes [16]. This leads to wider bandwidth and increased stability in the current measuring amplifier.

In section II, we will introduce the patch-clamp system. We will present the theory of series resistance compensation which increases the fidelity of the patch-clamp when recording large whole-cell currents. We will analyze the design of circuitry to remove the parasitic capacitive transients. In section III we will analyze the noise of the patch-clamp system. In section IV We will present the hardware test-bed developed to record data from patch-clamp experiments. In section V, experimental results of the patch-clamp system will be presented.

II. Patch-Clamp System Overview

Although our system is focused on an essential enabling technology, high-density planar electrode arrays such as those currently being developed by Molecular Devices and Sophion, a conventional patch-clamp setup that uses pipettes suffices to test the basic functionality of the integrated circuit. We predict from currently available data that the compensation settings are of similar magnitudes in both the conventional and planar electrode setups. Furthermore, adjusting these values to the necessary range will not be too difficult once massively parallel electrode arrays become available. Fig. 3 (A) shows a block diagram of our patch-clamp headstage with electrode compensation circuitry used in a conventional whole-cell patch-clamp experiment. The currents are typically a few nano amperes in amplitude with a bandwidth of 5-10 kHz. Our patch-clamp amplifier system consists of three main components: the *patch-clamp headstage* to monitor the membrane current, a *resistive compensation circuit* to compensate for the series resistance of the pipette and a *parasitic capacitive compensation circuit* to compensate for the current drawn by the electrode parasitic capacitance.

A. Patch-Clamp Headstage

The headstage monitors the cell membrane current while clamping the electrode at V_{com} using an operational amplifier. The membrane current I_{in} is recorded by an input current-to-voltage trans-impedance amplifier that uses resistive feedback (R_f). The non conductive substrate of SOS technology makes it possible to fabricate large resistors with minimal parasitic

TABLE I

DESIGN PARAMETERS OF THE INTEGRATED PATCH-CLAMP SYSTEM

Feedback Resistance, R_f	25MΩ
Feedback shunt capacitance, C_f	0.3pF
Injection capacitance , C_{inj}	10pF
Operational amplifier time constant, τ_{Amp}	0.05μs
Transconductor time constant, τ_z	7.5μs
Voltage clamp time constant, τ_{clamp}	0.8μs
Series resistance of the electrode, R_S (typical)	10MΩ

TABLE II

TYPICAL PARAMETERS IN A WHOLE-CELL PATCH-CLAMP EXPERIMENT

Total capacitance at the input, C_t (typical)	5-10pF
Parasitic capacitance at electrode, C_{prs} (typical)	3-5pF
Membrane resistance, R_m (typical)	10GΩ
Series resistance of the electrode, R_S (typical)	5-20MΩ
Cell membrane capacitance, C_m (typical)	10-100pF
Membrane access time constant, τ_a	50-2000μs
Pipette Membrane Seal Resistance (typical)	1-20GΩ
Membrane Current, I_m	±1-20nA

capacitance which increases speed, sensitivity and stability [16]–[19]. C_f is the shunt capacitance across the resistor. This shunt capacitance is necessary to make the trans-impedance amplifier stable and to increase the bandwidth of the voltage clamp. A difference amplifier subtracts the command voltage at which the membrane is clamped at from the trans-impedance amplifier's output. The difference amplifier was implemented as shown in Fig. 3 (B). The resulting output voltage is proportional to the input current and is low-pass filtered by the transconductor time constant $\tau_z = R_f C_f$, as shown in equation (1).

$$V_{out} = \frac{I_{in} R_f}{1 + \tau_z s} \tag{1}$$

The voltage clamp transfer function relating the pipette potential V_P to V_{clamp} shown in Fig. 3 is derived in equation (2). The operational amplifier is assumed to have a single pole located at τ_{Amp}. C_t is the total capacitance at the input.

$$V_p = \frac{V_{clamp}}{1 + \tau_{clamp} s} = \frac{V_{clamp}}{1 + \frac{C_t}{C_f}\tau_{Amp} s} \tag{2}$$

Using the parameters in Table II which lists typical parameters for a whole-cell recording experiment [15] as well as the parameters of our design listed in Table I, we calculate τ_z and τ_{clamp} to be 7.5μs and 0.8μs resulting in a transconductor bandwidth of 20kHz and a voltage clamp bandwidth of 180kHz respectively. Command voltage steps (V_{com}) between 0mV and 100mV are applied to the cell membrane during experiments, while recording the input currents. The device was designed to measure cell membrane currents up to ±20nA.

B. Series Resistance Compensation

The access resistance R_S to the cell is typically 5-20MΩ due the series resistance of the electrode. The capacitance of the cell membrane is about 10-100pF. The time constant associated with charging the cell membrane when a potential step V_{com} is applied to the electrode is several hundred microseconds. There is also a voltage error of tens of millivolts between the electrode potential V_P and membrane potential V_m due to the voltage drop across the series resistance since membrane currents I_m in the order of nano amperes are typical. Series resistance compensation is used to minimize this error.

In the series resistance compensation circuit shown in Fig. 3 (A), we estimate the voltage error caused by the access resistance and we make a correction to the command voltage, thereby effectively reducing the access resistance [15]. This reduction in series resistance enables us to voltage clamp the membrane accurately. It also reduces the time needed to charge the membrane capacitance C_m and enables the circuit to monitor ion-channel events occurring immediately after the control voltage is applied. The series resistance compensation circuit takes the current monitoring signal and scales it by a variable factor and adds it to the command voltage (V_{com}) in positive feedback polarity. A 9-bit digital setting K of the compensated resistance is applied to a multiplying digital to analog converter (mDAC) to control the amount of compensation. The series resistance compensation mDAC was designed to scale the current monitoring signal between 0.06-30 times with 9 bit resolution. A diagram of the 9 bit DAC is shown in Fig. 3 (C). The total output at the summing amplifier when switch SR_i is closed is given by equation (3) when RS_f was chosen as 10kΩ.

$$V_{RS} = -[\sum \frac{RS_f}{RS_i} \times V_{out} + V_{com}] \tag{3}$$

In our design, values of 612.5Ω, 1.25kΩ, 2.5kΩ, 5kΩ, 10kΩ, 20kΩ, 40kΩ, 80kΩ and 160kΩ were chosen for resistors RS_1-RS_9 respectively.

In order to derive the behavior of the V_m with V_{com} with series resistive compensation, we make the following assumptions. First, since τ_{clamp} is much shorter than the membrane access time constant τ_a (see Tables I and II), we will assume that V_{com} appears at V_P instantaneously. Second, we will assume that the membrane resistance R_m is very large compared to R_S and hence ignore it. The transfer function representation of this simplified system is shown in Fig. 4. The command voltage V_{com} is added to the compensation signal to yield the electrode potential V_p. A filtered version of this voltage with an access time constant τ_a=$R_S C_m$ appears at the membrane. The electrode current is the product of C_m and the time derivative of V_m. This current is converted to a voltage according to the transfer function of the trans-impedance amplifier. The resulting current monitoring voltage is then scaled by a factor K to yield the compensation voltage. The setting K can be written as in equation (4) where α is the fraction of R_S that is compensated. The entire closed loop transfer function relating V_m to V_{cmd} can then be written as in equation (5).

$$K = \alpha R_S \tag{4}$$

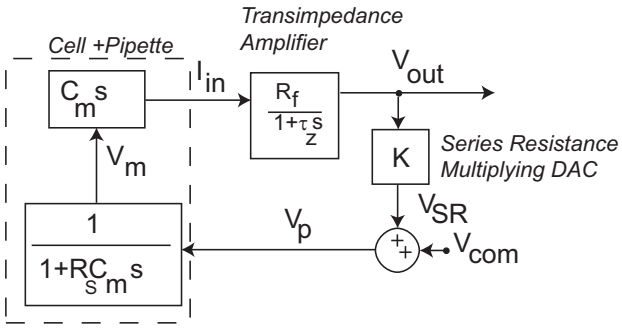

Fig. 4. Block model of the patch-clamp system with series resistance compensation.

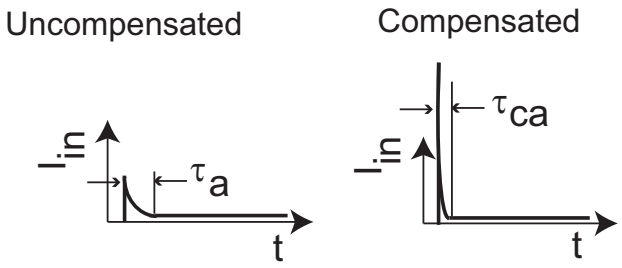

Fig. 5. The series resistance compensation circuit increases the system's bandwidth.

$$\frac{V_m}{V_{com}} = \frac{\tau_Z s + 1}{\tau_Z \tau_a s^2 + (1-\alpha)\tau_a s + 1} \tag{5}$$

$$\zeta = \frac{(1-\alpha)\sqrt{\frac{\tau_z}{\tau_a}}}{2} \tag{6}$$

$$\alpha \leq 1 - 2\sqrt{\frac{\tau_z}{\tau_a}} \tag{7}$$

The damping factor ζ of the second order transfer function in equation (5) can be written as in equation (6). When ζ drops below unity the output will overshoot. Therefore α is restricted to the range given in equation (7). The maximum level of compensation is limited by the bandwidth of the transconductor and also by the parasitic capacitance of the electrode as we will show in the next section. By substituting the values in Table I and II for τ_{clamp} and τ_a in equation (7) we would be able to compensate up to 70% of R_S (α_{max}=70%) and thereby see a three fold increase in bandwidth. This increase in bandwidth is illustrated in Figure 5. The time constant τ_{ca} associated with charging the membrane capacitance C_m through the compensated resistance (R_S-αR_S) is given by equation (8).

$$\tau_{ca} = C_m(R_S - \alpha R_S) \tag{8}$$

Therefore, when compensated, α approaches 1 and τ_{ca} decreases.

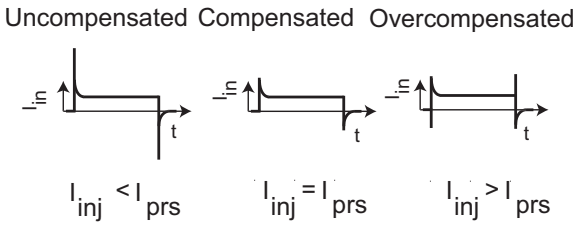

Fig. 6. The capacitive compensation circuit eliminates parasitic overshoots.

C. Parasitic Capacitive Compensation

The capacitive compensation circuitry shown in Fig. 3 (A) compensates for the current I_{prs} drawn by the parasitic capacitance of the electrode C_{prs} (see Table I) as well as other parasitic capacitances. The electrode capacitance is compensated by injecting a current I_{inj} through an integrated capacitor C_{inj} of 10pF. An 8-bit digital setting of AC_d is applied to a mDAC so that a range of C_{prs} values can be compensated.The implementation of the parasitic compensation mDAC shown in Fig. 3 (D) is similar to that of the series resistance compensation mDAC. The output of the inverting summing amplifier in the capacitive compensation mDAC is sent through an inverting unity gain buffer to obtain VC_c. When switches SC_i are closed, the output of the capacitive compensation mDAC is given by equation (9).

$$VC_c = \sum \frac{RC_f}{RC_i} \times V_{clamp} = AC_d \times V_{clamp} \tag{9}$$

In our design, RC_f was chosen as 10kΩ and values of 75Ω, 150Ω, 306Ω, 612.5Ω, 1.25kΩ, 2.5kΩ, 5kΩ, 10kΩ were chosen for resistors RC_1-RC_8 respectively, allowing parasitic capacitances up to 20pF to be compensated.

When the value of AC_d is set as given in equation (10) no parasitic current is drawn from the headstage and the parasitic capacitance is fully compensated.

$$(AC_d - 1)C_{inj} = C_{prs} \tag{10}$$

Fig. 6 shows the predicted response of the parasitic capacitance compensation circuit. When uncompensated, the headstage provides the currents needed to charge the parasitic capacitance. These 'fast' currents appear as narrow overshoots in the current monitoring signal with the same polarity as the control step. The 'fast' transients are superimposed on the slower transients associated with the time constant that charges the cell membrane, i.e. τ_a. When properly compensated, I_{prs} = I_{inj} and the overshoots do not appear. When overcompensated, $I_{inj} > I_{prs}$ and the overshoots appear negative.

The parasitic capacitance compensation prevents the electronics from saturating since it eliminates the need for the headstage to provide the large transient currents needed to charge the parasitic capacitances. An added benefit of capacitive compensation is that it reduces the effects of a noisy stimulus. In the same manner, that the parasitic currents caused by voltage steps are canceled, the compensation circuitry

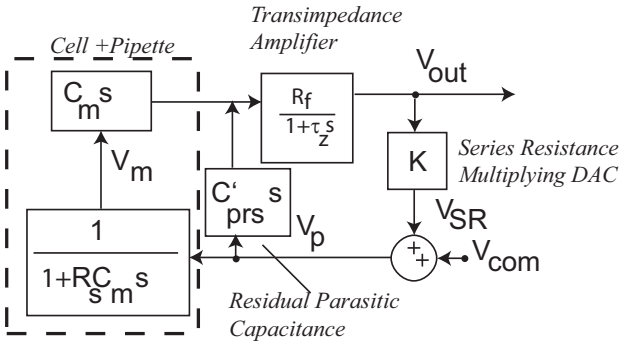

Fig. 7. Block model showing the effect of residual parasitic capacitance on series resistive compensation.

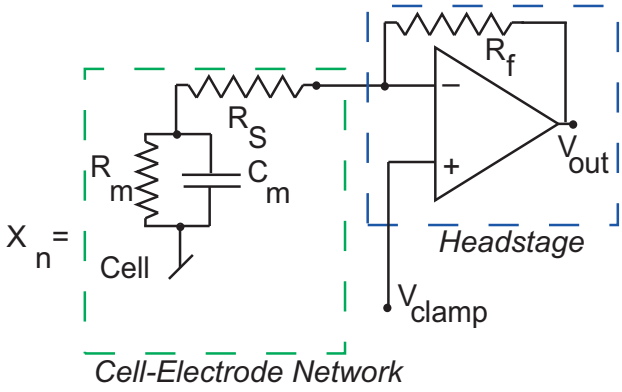

Fig. 8. Electrode plus cell network. The noise level of this network limits the performance of the patch-recording system.

cancels out the currents caused by noise in the stimulus voltage [15]. Furthermore, this technique increases the amount of applicable series resistance compensation. To understand why, let C'$_{prs}$ be the residual parasitic capacitance. The sign of C'$_{prs}$ could be either positive or negative depending on under-or over compensating respectively. The transfer function representation of the patch-clamp system with this residual parasitic capacitance included is shown in Fig.7. The transfer function derived in equation (5) can now be written as in equation (11). Positive C'$_{prs}$ adds phase lead to the R_S compensation loop introducing a damping effect and thereby stabilizing the compensation. However, excessively large values of C'$_{prs}$ increases the magnitude of the feedback and introduces oscillations. To prevent this, C'$_{prs}$ is kept smaller than τ_Z/R_S, i.e. about 0.75pF [15]. Therefore it is imperative that one cancels out the parasitic capacitance before performing series resistance compensation.

$$\frac{V_m}{V_{com}} = \frac{1}{(\tau_a s + 1)(-KZ_A C'_{prs} s + 1) - \tau_a K Z_A s} \tag{11}$$

III. Noise in the Patch-Clamp System

Low amplitude current measurements are often complicated by the presence of background noise. The background noise in patch-clamp measurements arise mainly from the electronic circuitry, and the cell-electrode network.

A. Cell-Electrode Noise in Patch-Clamp System

In whole-cell recording, usually the dominant background noise contributor is the cell-electrode network shown in Fig. 8 [20]. The noise level of cell plus electrode network, S_P can be calculated using equation (12) [21]. Here, K is the Boltzmann constant and T is the absolute temperature and X_N is the equivalent impedance of the pipette plus cell network. X_N can be calculated using equation (13). The current noise of the series combination of R_S and the membrane capacitance dominates in equation (12). The current noise of the membrane resistance can be ignored [20]. The current noise power spectrum of this simplified network is shown in equation (14).

$$S_P = \frac{4KT}{Re(X_N)} \tag{12}$$

$$X_N = \frac{R_m}{1 + R_m C_m s} + R_S \tag{13}$$

$$S_P = \frac{4KTR_S(2\pi f C_m)^2}{1 + (2\pi f R_S C_m)^2} \tag{14}$$

When designing a low-noise amplifier to measure low amplitude membrane current, it is sufficient to ensure that the noise contribution of the amplifier is less or comparable to S_P in the recording bandwidth.

B. Electronic Noise in the Patch-Clamp System

The electronic noise in the patch-clamp system arises primarily from the feedback resistor and the operational amplifier used to implement the I-V converter. The circuit model used to compute the electronic noise of the patch-clamp system is reported in Fig. 9. The total output voltage noise spectral density, S_V is given by equation (15). Y_c is resultant impedance at the input due to X_n, C_{prs} and C_{gs}. C_{gs} is the gate capacitance of the input transistor. The input-referred current noise spectral density S_I of the patch-clamp amplifier can be calculated by equation (16). e_M is the sum of the flicker noise and thermal noise components of the input transistor of the headstage and e_R is the thermal noise of the feedback resistor [22]–[24]. e_M and e_R can be calculated using equations (17) and (18) respectively.

$$S_V = e_M^2 + e_R^2 + e_M^2 Y_c^2 {R_f}^2 \tag{15}$$

$$S_I = \frac{S_V}{{R_f}^2} = \frac{e_M^2 + e_R^2}{{R_f}^2} + e_M^2 Y_c^2 \tag{16}$$

$$e_M^2 = C_T + \frac{C_F}{f} \tag{17}$$

$$e_R^2 = 4KTR_f \tag{18}$$

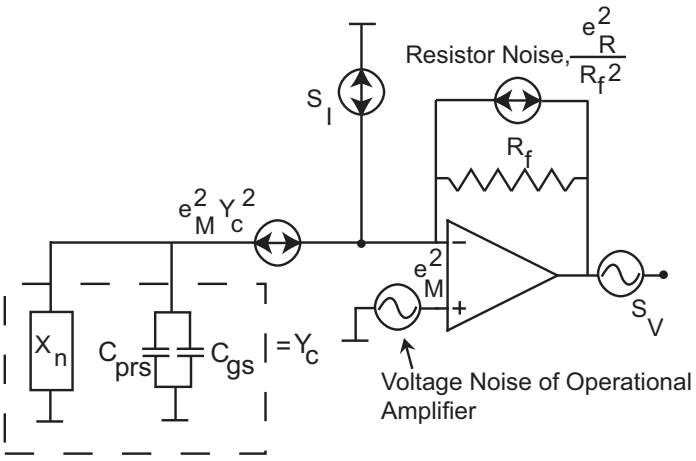

Fig. 9. The model used to calculate the electronic noise of the patch-clamp.

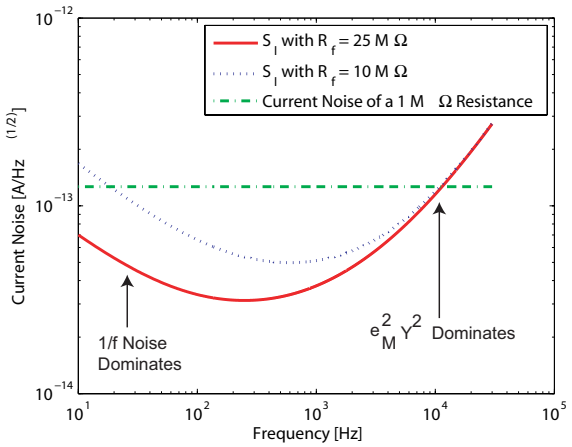

Fig. 10. Electronic noise of the unloaded patch-clamp headstage. The current noise spectral density S_I is dominated by 1/f noise at low frequencies and at higher frequencies by the voltage noise that is reflected on the input impedance. S_I has an inverse relationship with the feedback resistance R_f. When using a R_f of 25MΩ, the value of S_I at 5kHz is comparable to the current spectral density of a 1MΩ resistance.

$$SI_{Tot} = S_I + S_P \tag{19}$$

Here C_F is the process dependant flicker noise coefficient and C_T is the thermal noise coeffircient of the input transistor (see Table III). The total input referred current spectral density, SI_{Tot} of the patch-clamp system is given by equation (19). Fig. 10 shows S_I, the theoretical unloaded noise of the patch-clamp amplifier, plotted using equation (16). The flicker noise component of the noise dominates S_I at low frequencies. At higher frequencies, S_I is dominanted by the voltage noise that is reflected Y_c. The current noise at the input decreases with R_f. However the physical size of of R_f in layout as well the headroom limitations in the amplifier limits its value. A R_f of 25MΩ was chosen for our design. When using a R_f of 25MΩ, the value of S_I at 5kHz is comparable to the current spectral density of a 1MΩ resistance. The current noise spectral density S_P of the cell-electrode network is compared with SI_{Tot} in Fig. 11. S_P is the dominant component of SI_{Tot} in the recording bandwith.

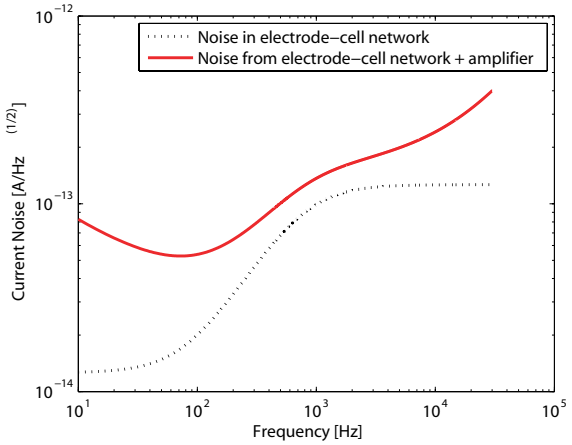

Fig. 11. Current noise spectral density, S_P of the electrode-cell network compared with the total input referred current noise spectral density, SI_{Tot}. S_P is the dominant component of SI_{Tot} in the recording bandwith.

C. Noise in the Operational Amplifier

The patch-clamp technique is extremely sensitive to noise due to the low amplitude of the membrane current and hence low-noise amplification is critical to our design. All amplifiers are implemented using a low-noise three stage operational amplifier shown in Fig. 12. The input transistors are vital in establishing the noise characteristics of the operational amplifier. The gate capacitance C_{gs} of the input MOSFET is proportional to the area of the transistor, while the thermal noise e_n decreases as the square root of the area (assuming constant gate length). The noise of the recording system is proportional to $C_{in}e_n$ where the total input capacitance is C_{in} = C_g + C_{prs}. A [W/L] ratio of [15/5] was used in our design. The characteristics of the operational amplifier are summerized in Table III.

TABLE III

PERFORMANCE OF THE OPERATIONAL AMPLIFIER USED IN THE DESIGN

DC Gain	72dB
Gainbandwidth Product	3MHz
Input common mode range	$0.5V_{pp}$
Output swing	$0.7V_{pp}$
Slew rate	3.3V/μs
Bias current at 3.3V	20μA
Flicker noise coefficient, C_F	$2.6x10^{-11}V^2$
Thermal noise coefficient, C_T	$2.4x10^{-15}$ V^2/Hz

IV. HARDWARE TEST-BED

A diagram of the hardware test-bed is shown in Fig. 13. The entire system is powered at 3.3V using a USB bus and

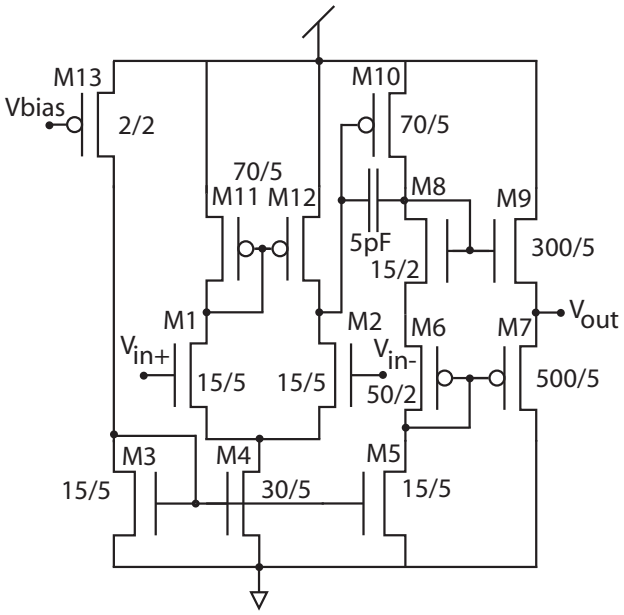

Fig. 12. The operational amplifier used in the design. All ratios [W/L] are given in micron. RN and RP type transistors were used in the design.

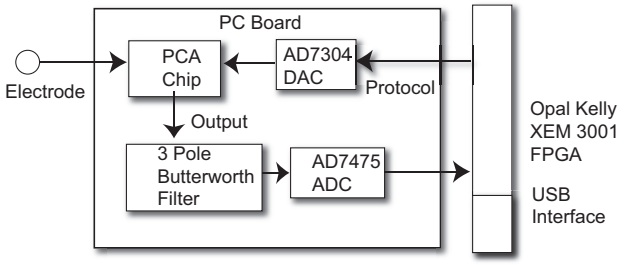

Fig. 13. A block diagram of the harware test-bed. The test-bed consists of an ADC, a DAC and an anti aliasing filter. The patch-clamp system is controlled using a GUI driven C++ program.

the digital interface was provided using a field programmable gate array on an Opal Kelly 3001 board. The command voltage was provided by an Analog Instruments 8 bit AD7304 digital to analog converter (DAC). The output of the amplifier was digitized using a 12 bit Analog Instruments AD7475 analog to digital converter. The data was sampled at 62.5kHz and low-pass filtered at 20kHz using a three pole butterworth filter. A GUI driven C++ program allows the compensation mDACs to be set, stimulus pulses to be generated and the current signals to be plotted. The entire system consists of two stacked circuit boards and was packaged in a shielded box.

V. Experimental Results

Fig. 14 shows recordings of ion-channel activations made from our patch-clamp system on Human Embryonic Kidney 293(HEK) cells expressing expressing hslo channels (calcium-activated potassium channels). The measurements were made using a conventional patch-clamp setup. The bath solution contained 150mM KCl, 40 μM $CaCl_2$ and 10mM HEPES

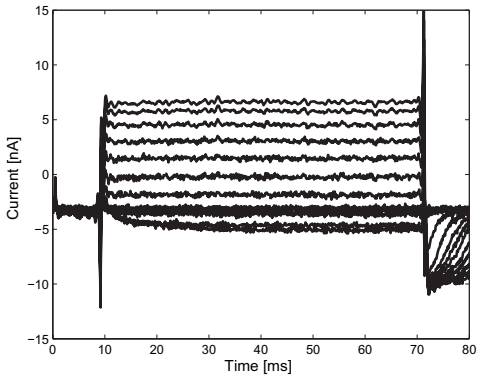

Fig. 14. Ion channel activation in HEK cells expressing a high density of hslo channels carrying K+ current.

while the pipette solution contained 16mM KCl, 144mM NaCl and 10mM HEPES. The bath was held at ground potential while depolarizing command voltage (V_{com}) steps were applied in steps of 15 mV from -150 to +60 to the membrane. The holding potential of the membrane was -100mV. The traces were filtered at 5kHz for display. The steady state I-V curve is shown in Fig. 15. The ion-channels start to activate when the membrane potential is less than the holding potential (-100mV). The currents are at first negative and increase in magnitude when more channels activate as the membrane potential increases. The currents turn positive when the applied potential is in the vicinity of -60mV. This value conforms with the 'reversal potential' E_R, calculated using Nernst equation shown in (20) which is governed by the laws of thermodynamics [25]. Here $[K]_b$ is the free potassium ion concentration in the bath (150mM) and $[K]_p$ is the free potassium concentration in the pipette (16mM). Fig. 16 shows the glass micropipette electrode (1μm diameter tip) and the HEK cells used to make the recordings.

$$E_R = -60log_{10}\frac{[K]_b}{[K]_p} \tag{20}$$

Fig. 17 shows the measured step responses of the patch-clamp system while using series resistance compensation. As prediced by equation (7) and Fig. 5 we were able to decrease the time constant needed to charge cell membrane from 600μs to 200μs obtaining a threefold increase in bandwidth. This corresponds to compensating 70% of a 4MΩ series resistance.

Fig. 18 shows the measured response of the patch-clamp system while using parasitic capacitance compensation. As predicted from equation 10 and Fig. 6 we were able to see positive, negative and no overshoots corresponding to undercompensation, overcompensation and proper compensation of the parasitic capacitance. The shown response is for approximately 10pF of parasitic capacitance at the input. We were able to compensate up to 20pF of parasitic capacitance.

Fig. 19 shows the measured input-referred current noise spectrum compared with the theoretical noise as calculated

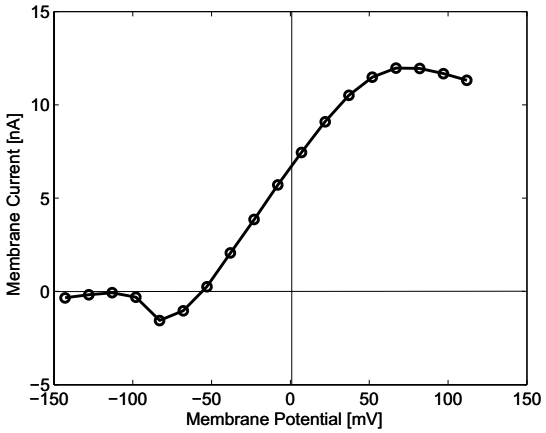

Fig. 15. Steady state membrane current to voltage relationship when depolarizing steps are applied across the cell membrane. The measured reversal potential value conforms with the theoretical value calculated using Nernst equation.

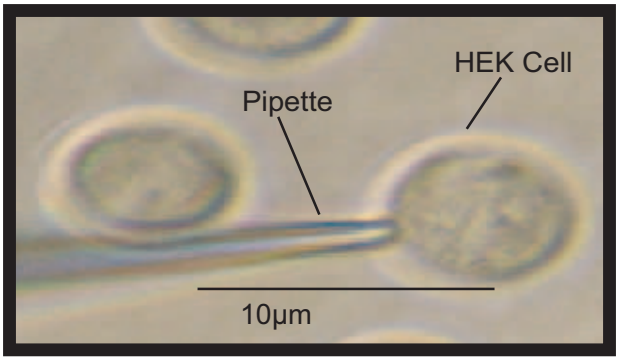

Fig. 16. Human embryonic kidney cells and glass micropipette.

in equation (16). Integrating the input-referred noise yields an rms current noise of 5pA at 10kHz bandwidth. This corresponds to a signal-to-noise ratio of 250 or approximately 8 bits in whole-cell patch-clamp measurements when the input is 1nA. This result is comparable to state-of-the-art commercially available bench-top amplifiers made with discrete componenets. For example, the ionWorks Quattro amplifier from Molecular Devices has noise levels of 10pA of rms current at 10kHz bandwidth [26]. The Triton-1 device from Tecella technologies has 0.5pA rms at 3kHz bandwidth while using a R_f value of 1GΩ [27].

TABLE IV
PERFORMANCE OF THE PATCH-CLAMP SYSTEM

Process technology	SOS 0.5μm CMOS
Input referred current noise at 10KHz	5pA$_{rms}$
Signal to noise ratio with 1nA input	250
Resistive compensation capability	70% of 4MΩ
Capacitive compensation capability	20pF
Power consumption at 3.3V	300μW
Chip area (with pads)	1150μm x 700μm

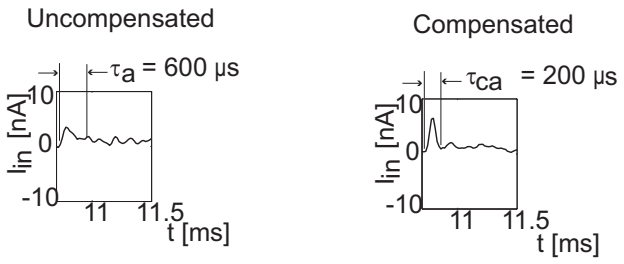

Fig. 17. Measured response of the series resistance compensation circuit. The circuit is able to compensate for up to 70% of 4MΩ series access resistance.

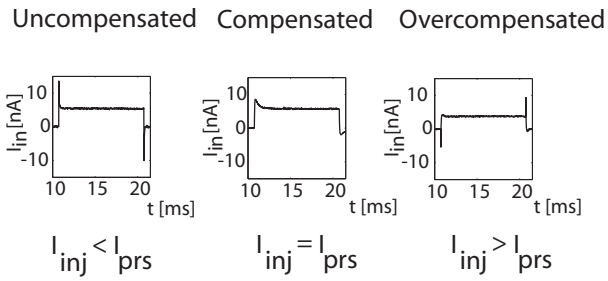

Fig. 18. Measured response of the capacitive compensation circuit. This response was obtained while the circuit compensated a 10pF parasitic capacitance.

The power consumption of the patch-clamp system was measured as 300μW with a 3.3V power supply. The power consumption is dominated by the five operational amplifiers used in trans-impedance and differene amplifiers and the resistive and parasitic capacitive compensation mDACs. Each operational amplifier consumes 20μA of bias current. The performance of the patch-clamp system is summerized in Table IV. The prototype was fabricated in a 0.5μm silicon-on-sapphire process. The die size is 1150 by 700μm. The power consumption is 300μW at 3.3V. A micrograph of the fabricated die is shown in Fig. 20.

VI. SUMMARY

We designed, fabricated and tested an integrated patch clamp amplifier with series resistance and parasitic capacitive compensation circuitry targeting high throughput patch-clamp systems using planar electrodes. The device uses a trans-impedance amplifier to convert an input current to a voltage output. The system can record cell membrane currents up to ±20nA, with a rms noise of 5pA at 10kHz bandwidth. The system can compensate for the capacitance and resistance of the electrode, up to 20pF and 70% of the series access resistance respectively. The performance of the prototype integrated patch-clamp system is comparable with the commercial bench-top systems. However, due to its greatly smaller size, the integrated system will be an essential enabling technology to build massively-parallel amplifier arrays, for the next generation of high-density patch-clamp systems.

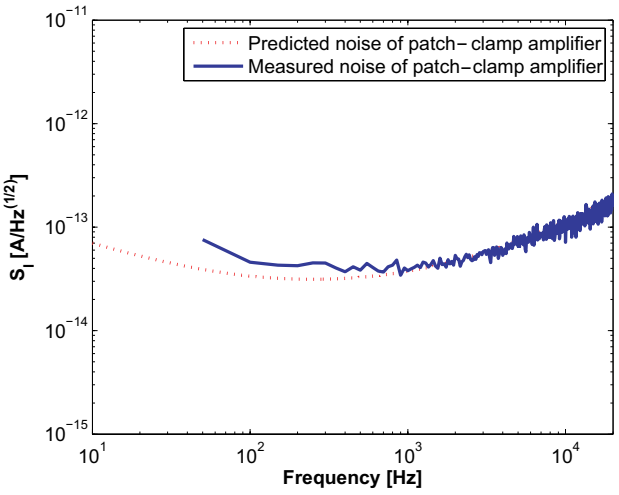

Fig. 19. Measured amplifier input-referred current noise spectral density compared with the theoretical value calculated in equation 16. Integrating the input noise curve yields a rms noise current of 5pA.

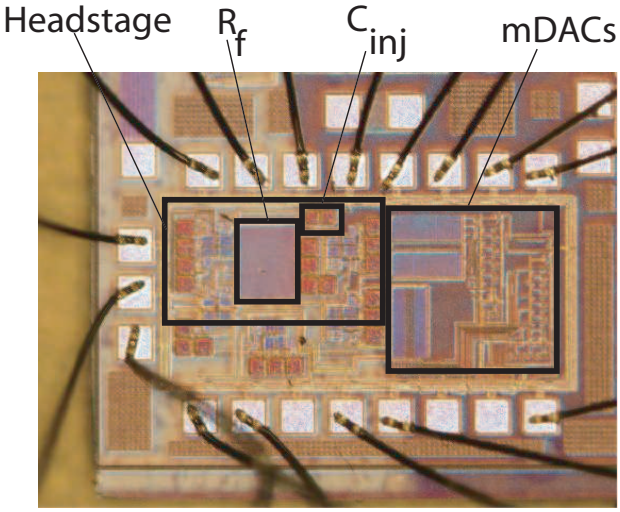

Fig. 20. Die micrograph of the integrated patch-clamp amplifier

VII. Acknowledgements

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References

[1] D. Roden, "Drug-induced prolongation of the QT interval," *New England Journal of Medicine*, vol. 350, pp. 1013 – 1022, 2004.

[2] O. Hamill, A. Marty, E. Neher, B. Sakmann, and F. Sigworth, "Improved patch-clamp technique for high-resolution current recording from cells and cell-free membrane patches," *European Journal of Physiology*, vol. 391, pp. 85–100, 1981.

[3] F. J. Sigworth, "Life's transistors," *Nature*, vol. 423, pp. 21–22, May 2003.

[4] N. Fertig, R. Blick, and J.C.Behrends, "Whole cell patch clamp recording performed on a planar glass chip," *Biophys J.*, vol. 82, pp. 3056–3062, June 2002.

[5] N. Fertig, A. Tilke, R. Blick, and J. Behrends, "Nanostructured suspended aperture for patch clamp recording and scanning probe application on native membranes," *Biophys. J.*, vol. 78, 2000.

[6] A. Brueggemann, M. George, M. Klau, M. Beckler, J. Steindl, J. Behrends, and N. Fertig, "Ion channel drug discovery and research: The automated nano-patch-clamp technology," *Current Drug Discovery Technologies*, vol. 91, pp. 91 – 96, 2004.

[7] S. Pandey and M. H. White, "An integrated planar patch-clamp system," in *International Semiconductor Device Research Symposium*. IEEE, December 2001, pp. 170–173.

[8] H. Narula and J. Harris, "A time-based VLSI potentiostat for ion current measurements," *IEEE Sensors Journal*, vol. 6, no. 2, pp. 239–247, 2006.

[9] F. Sigworth and K. Klemic, "Microchip technology in ion-channel research," *IEEE Transactions On Nanobioscience*, vol. 4, no. 1, pp. 121–127, 2005.

[10] S. Ayers, K. Gillis, M. Lindau, and B. Minch, "Design of a CMOS potentiostat circuit for electrochemical detector arrays," *IEEE Transactions On Circuits and Systems*, vol. 54, no. 4, pp. 736–743, 2007.

[11] F. Laiwalla, K. Klemic, F. Sigworth, and E. Culurciello, "An integrated patch-clamp amplifier in silicon-on-sapphire CMOS," in *IEEE International Symposium on Circuits and Systems, ISCAS '06*. Kos, Greece: IEEE, May 2006, pp. 4054–4057.

[12] P. Weerakoon, K. Klemic, F. Sigworth, and E. Culurciello, "An integrated patch-clamp amplifier for high-density whole-cell recordings," in *IEEE International Symposium on Circuits and Systems, ISCAS '07*. New Orleans, LA: IEEE, May 2007, pp. 1205–1209.

[13] R. Genov, M. Stanacevic, M. Naware, G. Cauwenberghs, and N. Thakor, "16-channel integrated potentiostat for distributed neurochemical sensing," *IEEE Transactions on Circuits and Systems*, vol. 53, no. 11, pp. 2371–2376, November 2006.

[14] M. Stanacevic, K. Murari, A. Rege, G. Cauwenberghs, and N. Thakor, "VLSI potentiostat array with oversampling gain modulation for wide-range neurotransmitter sensing," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 1, no. 1, pp. 63–72, March 2007.

[15] B. Sakmann and E. Neher, Eds., *Electronic Design of the patch-clamp*. Plenum Press, February 1995, ch. 1, F.J Sigworth.

[16] Peregrine, *0.5um FC Design Manual*, 52nd ed., Peregrine Semiconductor Inc., San Diego, CA, March 2008.

[17] S. Cristoloveanu and S. S. Li, *Electrical Characterization of Silicon-On-Insulator Materials and Devices*. Kluwer Academic Publishers, 1995.

[18] J. B. Kuo and K. W. Su, *CMOS VLSI Engineering Silicon-on-Insulator (SOI)*. Kluwer Academic Publishers, 1998.

[19] A. G. Andreou, Z. K. Kalayjian, A. Apsel, P. Pouliquen, R. A. Athale, G. Simonis, and R. Reedy, "Silicon on sapphire CMOS for optoelectronic microsystems," *IEEE Circuits and Systems Magazine*, vol. 1, no. 3, pp. 22 – 30, 2001.

[20] E. Neher and B. Sakmann, Eds., *Whole-Cell Recording*. Plenum Press, February 1995, ch. 7, A Marty and E Neher.

[21] J. Johnson, "Thermal agitation of electricity in conductors," *Physical Review*, vol. 32, no. 7, pp. 97–109, July 1928.

[22] R. Sarpeshkar, T. Delbruk, and C. Mead, "WHITE noise in MOS transistors and resistors," *IEEE Circuits and Devices Magazine*, pp. 23–29, November 1993.

[23] Y. Nemirowsky, I. Brouk, and C. Jacobson, "1/f noise in CMOS transistors for analog applications," *IEEE Transactions On Electronic Devices*, vol. 48, no. 5, pp. 921–927, 2001.

[24] R. Kansy, "Response of a correlated double sampling circuit to 1/f noise," *IEEE Journal of Solid-State Circuits*, vol. 15, no. 3, pp. 373–375, June 1980.

[25] B.Hille, Ed., *Ion Channels of Excitable Membranes*. Sinauer, 2001, ch. 1, B. Hille.

[26] Molecular Devices Electrophysiology Instruments, "Url http://www.moleculardevices.com/."

[27] Tecella Electrophysiology Instruments, "Url http://www.tecella.com/."