

A Low-Power High-Speed Ultra-Wideband Pulse Radio Transmission System

Wei Tang, *Student Member, IEEE*, and Eugenio Culurciello, *Member, IEEE*

Abstract—We present a low-power high-speed ultra-wideband (UWB) transmitter with a wireless transmission test platform. The system is specifically designed for low-power high-speed wireless implantable biosensors. The integrated transmitter consists of a compact pulse generator and a modulator. The circuit is fabricated in the 0.5- μm silicon-on-sapphire process and occupies 420 $\mu\text{m} \times 420 \mu\text{m}$ silicon area. The transmitter is capable of generating pulses with 1-ns width and the pulse rate can be controlled between 90 MHz and 270 MHz. We built a demonstration/testing system for the transmitter. The transmitter achieves a 14-Mb/s data rate. With 50% duty cycle data, the power consumption of the chip is between 10 mW and 21 mW when the transmission distance is from 3.2 to 4 m. The core circuit size is 70 $\mu\text{m} \times 130 \mu\text{m}$.

Index Terms—Implantable biosensors, low-power high-speed UWB transmitter, pulse generator, pulse modulation, ultra-wideband radio (UWB), wireless biomedical applications.

I. INTRODUCTION

RECENT years have seen an increasing demand in wireless communication technology for sensor nodes [1]. Particularly in implantable biosensor applications, a high-speed low-power wireless transmitter is a significant technical hurdle. A traditional radio-frequency (RF) circuit (with less than a 1-Mb/s data rate) and optical transcutaneous transmission (higher than 100-mW power cost) are not ideal candidates in this case. A 100-channel biopotential recording system requires a transmitter design with at least a 13-Mb/s data rate and less than 10-mW power consumption [2].

Ultra-wideband (UWB) pulse radios have the potential to satisfy these requirements. A UWB pulse radio is a kind of wireless transmission whose output occupies a wide frequency spectrum. A radio system is considered to be of the UWB kind when its fractional bandwidth is greater than 0.25 or occupies a spectrum of at least 0.5 GHz [3]. A UWB transmitter is based on the modulation of pulses and does not use a carrier. It can be designed to have a high-data rate and low power consumption [4]. Due to these reasons, UWB is used for indoor communications, personal communications [1], wireless sensor networks [5], body-area networks [6], [7] and neural recording systems [8].

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The authors are with the Electrical Engineering Department, Yale University, New Haven, CT 06520 USA (e-mail: wei.tang@yale.edu; eugenio.culurciello@yale.edu).

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Aside from the high data rate and low power transmission, the UWB radio has many advantages for biomedical applications [9]. First, UWB has low electromagnetic (EM) radiation due to the low transmitted power, which makes it safe for tissue and the human body. Second, the UWB transmitter is a compact circuit with low complexity and small silicon area and, thus, can be easily added to the design of implantable biosensors. Third, UWB radios can use multiple pulses to represent one symbol, so they can obtain the same high gain of conventional spread-spectrum radios. This increases its capability of penetrating through obstacles [10]. These features are very important in biomedical applications.

The pulse generator is the fundamental block of a UWB transmitter. The speed and power performance are essential parameters to characterize a UWB pulse generator. UWB transmitters are known as low-complexity and low-power circuits. However, in previous designs, the oscillator, pulse generator, and modulator were separate components [4], [11], which increases the design complexity, silicon area, and power consumption. One transmitter implementation in a 0.13- μm process [12] consumes 350- μW energy with a 10-MHz data rate, occupying a 0.48 mm^2 chip area. Another pulse generator in a 0.18- μm process [13] has a 100-MHz rate, 18.33-mW power consumption, and 0.078 mm^2 area.

In our design, the oscillator, pulse generator, and modulator are merged in a compact circuit, which can be easily adapted as a short-range wireless module. The pulse generator occupies 70 by 130 μm of area on the chip and offers a power consumption of less than 1 mW with a 270 MHz f_p . We have designed and implemented a complete pulse-based communication system with a 14-Mb/s data rate and 10- to 21-mW average power consumption depending on transmission distance. The device is ideally suited for implantable biopotential recording systems.

This paper is organized as follows. Section II describes the pulse generator circuit, the architecture of the transmitter, antenna design, and wireless transmission system. Section III presents the test results from the fabricated integrated circuit (IC). Section IV describes the experimental results of the wireless transmission system. Finally, Section V summarizes the paper.

II. SYSTEM OVERVIEW

A block diagram of the transmitter is reported in Fig. 1. The transmitter is an IC which consists of a pulse generator and an amplitude modulator. The discrete-components receiver includes a commercial RF detector and a digitizer. The pulses from the pulse generator are modulated and transmitted to the RF detector wirelessly through the antennas. In this paper, the pulse generator and amplitude modulator are designed

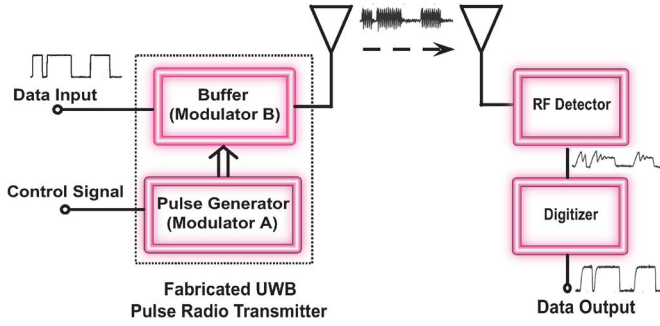


Fig. 1. Block diagram of the UWB transmission system with typical waveforms at different nodes. The integrated transmitter is composed of a pulse generator and an output buffer. The pulse generator and the buffer can be used as pulse modulators. The discrete-component receiver consists of an RF detector and a digitizer.

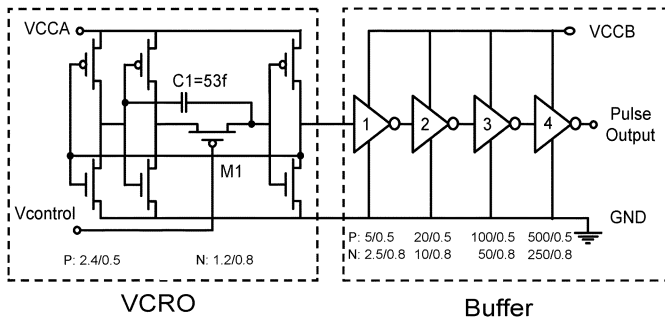


Fig. 2. Schematic of the integrated UWB pulse generator. It contains a voltage-controlled ring oscillator (VCRO) as the pulse generator and an output buffer. The MOSFETs in the VCRO are of minimum size. The width and length sizes (W/L) of PMOSs and NMOSs are illustrated in the figure. P is for PMOS and N is for NMOS.

and fabricated on-chip. Commercial chips are used in the Rx node. They are the ADL5513 (Analog Devices, Inc.) as the RF detector and the LMV7239 (National Semiconductor) as the digitizer.

1) *Pulse Generator and Transmitter*: In previous realizations, two methods are used to generate a pulse. They are the inverter delay method and the high-pass filter method [4]. In this design, we combine the two methods in one unit to form a compact pulse generator. The schematic of our pulse generator is shown in Fig. 2. It consists of two components: 1) a voltage-control ring oscillator (VCRO) as a pulse generator and 2) an output buffer as a modulator. The VCRO is implemented with a three-stage inverter-based ring oscillator with an internal RC high-pass filter. Our design saves silicon area because multiple functions are combined: the pulse generator also works as a modulator to control the pulse rate. The output stage is implemented with four inverters to buffer the pulse generator output and provide enough transmitter power to transmit up to 4 m. The pulse repetition rate can be controlled by VCCA (shown in Fig. 2) and V_{control} . VCCA controls the oscillation frequency by changing the supply voltage of the oscillator. C1 and M1 implement a variable filter that can change the oscillation frequency by means of V_{control} . The drain current of M1 charges C1, the charging and discharging time affect the frequency. When VCCA is connected to the power supply and V_{control} is connected to ground, the pulse generator has the maximum f_p .

The charging time (T1) and discharging time (T2) of C1 can be estimated in (1) and (2), where V_{thn} and V_{thp} are the threshold voltages of the NMOS and PMOS (M1). R is the equivalent resistor of M1 during the transition. The first-order approximation of the PMOS resistance in the linear region is shown in (3). μ_0 is the carrier mobility. ϵ_{SiO_2} and t_{ox} are the dielectric permittivity and thickness of the gate oxide in M1, respectively. W and L are the channel width and length. The metal-oxide semiconductor field-effect transistors (MOSFETs) in the VCRO are in the minimum size. In PMOS, the W and L are 2.4 μm and 0.5 μm . In NMOS, the W and L are 1.2 μm and 0.8 μm . Assuming the average V_{gs} during the transition is $1/2$ VCCA (with V_{control} connected to ground), the relationship of f_p and VCCA is represented as

$$T1 = RC_1 \ln \frac{VCCA}{V_{\text{thn}}} \quad (1)$$

$$T2 = RC_1 \ln \frac{VCCA}{V_{\text{thp}}} \quad (2)$$

$$R = \frac{1}{\mu_0 \frac{\epsilon_{\text{SiO}_2}}{t_{\text{ox}}} \left(\frac{W}{L}\right) (V_{\text{gs}} - V_{\text{thp}})} \quad (3)$$

$$f_p = \frac{1}{T1 + T2} = \frac{\mu_0 \frac{\epsilon_{\text{SiO}_2}}{t_{\text{ox}}} \left(\frac{W}{L}\right) \left(\frac{1}{2} VCCA - V_{\text{thp}}\right)}{C_1 \ln \frac{VCCA^2}{V_{\text{thp}} V_{\text{thn}}}} \quad (4)$$

VCCB can be used as a pulse-output enable signal, as well as a bias to control the pulse amplitude and transmitted power. The output pulse amplitude and total power consumption will decrease with VCCB. The number of the stages and the size of each device in the output buffer are designed to match and drive the antenna load according to the power budget. The output buffer dominates the power consumption of the integrated UWB pulse radio transmitter. In our design, the buffer has four stages that can provide a maximum of 42 mW (at the maximum pulse repetition rate) with a 3.3-V power supply, to drive the load of the pad, bonding wire, and antenna. The average power cost is 10-21 mW (depending on transmission distance) with 50% duty cycle data.

2) *Antenna Design*: The antenna is another key component for the UWB transmission system [14]. It should be able to transmit wideband signals with minimum distortion in order to keep the pulse shape and amplitude in the time and frequency domains [15]. Generally, a tapered triangle-shaped antenna is used in a wideband transmission system [16]. In our design, we implemented the transmitter on a 1.8 \times 0.9 in. printed-circuit board (PCB) with an onboard triangular antenna. We used another planar triangular copper foil as a receiver antenna. The transmission distance is up to 4 m. A picture of the transmitter board and receiver antenna is shown in Fig. 3. The antenna pair is sufficient for the objectives defined in this paper. A 0.5-in. metal monopole wire antenna was tested in our testing system. This wire antenna suppresses the transmission distance of up to 0.8 m. The received spectrum from different antennas is compared in Section IV.

3) *Wireless Transmission System Design*: We developed the software and a full hardware prototype to test the wireless communication. The UWB pulse-radio transmission system block diagram with photographs of the demonstration/testing system

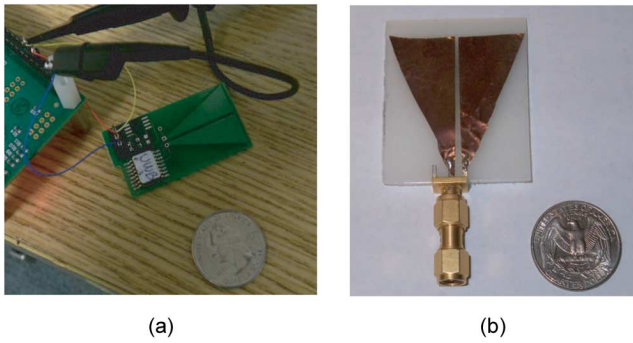


Fig. 3. (a) Transmitter is implemented on a 1.8×0.9 -in PCB with an onboard antenna. (b) The receiver antennas in our design are triangular copper foil on a plastic sheet. The full size is 2×1.5 in.

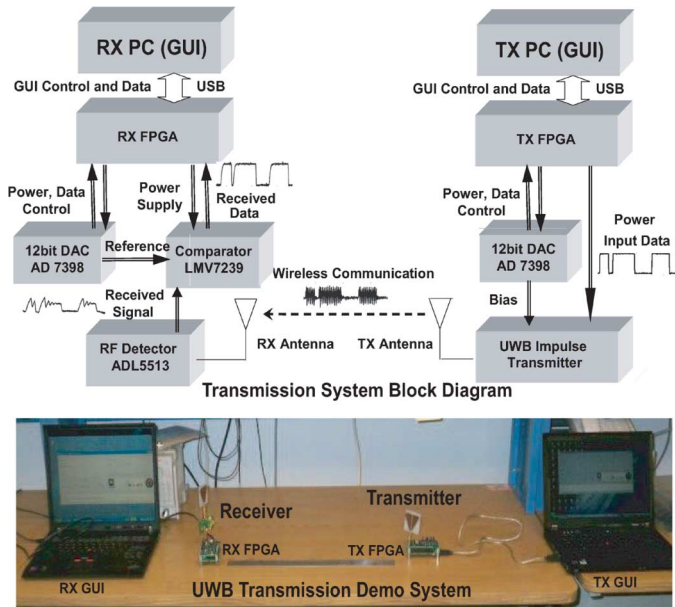


Fig. 4. UWB impulse radio wireless transmission demonstration/testing system with typical waveforms at different nodes. The input data are delivered from the PC to the FPGA by a universal serial bus. The Tx FPGA provides the power supply and the input data. The RF detector received the pulses from the transmitter. The data are recovered by a comparator and sent to the Rx FPGA. The system is controlled by a graphic user interface (GUI).

is shown in Fig. 4. In this system, data are sent from one computer to the UWB pulse-radio transmitter through the Tx field-programmable gate-array (FPGA) board. The UWB pulse-radio transmitter converts the data into a sequence of pulses and transmits them through antennas. The pulses are received by an RF detector, and converted to a digital signal by means of a comparator in the receiver. The received data are recorded back to the computer through the receiver (Rx) FPGA. We use a 12-bit digital-to-analog converter (DAC) (AD7398, Analog Devices, Inc.) to provide bias voltages for the transmitter and comparator circuits. The system utilizes a graphic user interface (GUI) to control the biases and transmission data rate. With the GUI one can select, send, and receive a file between two computers through the UWB pulse-radio system.

III. IC TEST RESULT

Our prototype was fabricated on Peregrine Semiconductors' $0.5\text{-}\mu\text{m}$ silicon-on-sapphire (SOS) complementary metal-oxide

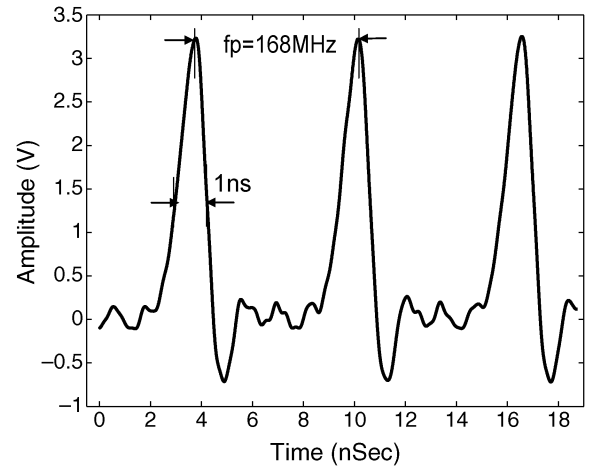


Fig. 5. Output pulses generated by our integrated UWB transmitter. Three pulses are shown with amplitudes of 3.3 V. The duration of each pulse is 1 ns. V_{control} was set to ground and the pulse frequency (f_p) is 168 MHz.

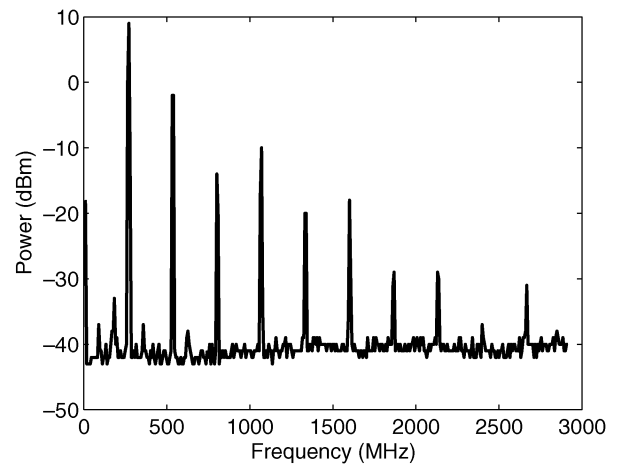


Fig. 6. Measured power spectrum density of the pulse generator with buffer. The spectrum contains high-frequency components up to 3 GHz. The first peak (270 MHz) is the pulse repetition rate. Eighty-five percent of the energy is in the first three peaks.

semiconductor (CMOS) process and packaged in a DIP16 package. We chose the SOS technology for its speed and low-power operation and its isolating substrate. This substrate offers lower parasitic capacitance than a bulk CMOS circuit, and 30% faster speed than the same feature size bulk CMOS process [17]. The total area of the IC without pads is $70 \mu\text{m} \times 130 \mu\text{m}$ and $420 \mu\text{m} \times 420 \mu\text{m}$ with pads. The normal power supply of the circuit is 3.3 V.

We tested the integrated UWB pulse generator with an Agilent 54845A 2 GHz oscilloscope and a 0.5-pf load active probe. The measured waveform of the transmitter is illustrated in Fig. 5, where three pulses are shown. The on-chip pulse generator generates pulses of 1-ns duration (at 50% to 50% of the amplitude). The pulse amplitude is 3.3 V. The frequency of the pulses (f_p) can be controlled by V_{CCA} or V_{control} .

The power spectrum density of the UWB pulse radio transmitter is illustrated in Fig. 6. The input data are set to "1." The first peak at 270 MHz is the f_p . The spectrum contains high-frequency components up to 3 GHz. Eighty-five percent of the

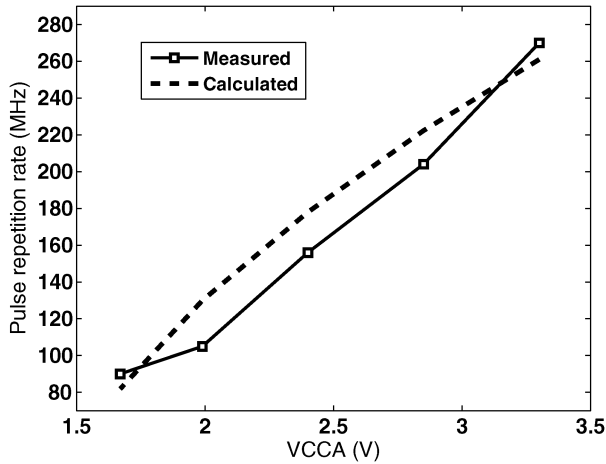


Fig. 7. Measured and calculated pulse frequency as a function of VCCA. The pulse frequency increases with VCCA.

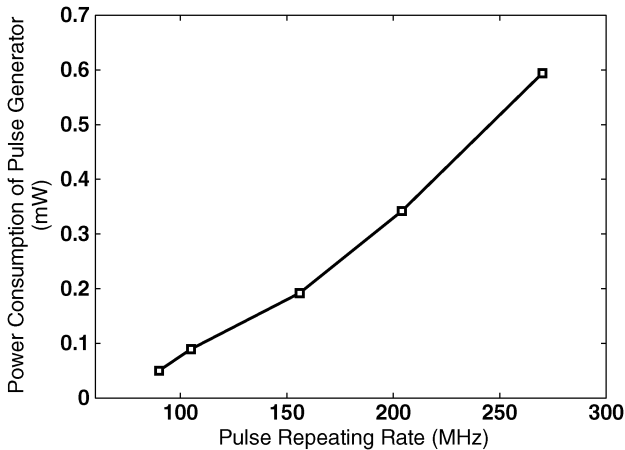


Fig. 8. Measured power consumption of the pulse generator at a different pulse rate (f_p).

transmitted energy is in the first three spectral peaks; therefore, most of the energy is located below 600 MHz, which is similar to the other wireless biosensor system [2]. Signal attenuation by the environment at this frequency should not affect the system in short-range transmissions. We performed a mock-implanted system test by immersing Rx and Tx antennas in a water phantom (water tank). The resulting attenuation due to the water was negligible.

Fig. 7 shows the test and calculated results of pulse frequency modulation with VCCA. The calculation is based on (4) and the BSIM parameters of the SOS process. The charging and discharging time of $C1$ is affected by the current in $M1$, which is a function of VCCA. The period of pulses will increase if VCCA decreases. When VCCA is 1.6 V, the f_p is 90 MHz. The maximum f_p is achieved when VCCA is connected to the power supply (3.3 V), then the rate is 270 MHz.

We measured the frequency and power consumption of the pulse generator with a 3.3-V power supply. The results are shown in Fig. 8. When changing VCCA from 1.6 V to 3.3 V, f_p increases from 90 MHz to 270 MHz. The VCRO is always on and its power consumption is 50 μ W when the pulse rate is 90 MHz, and 0.6 mW when the pulse rate is

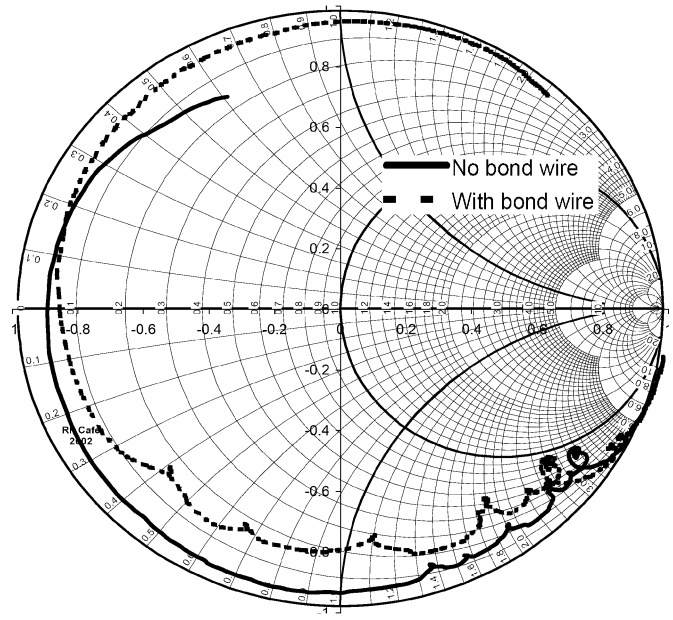


Fig. 9. Measured S11 parameter of the antenna in Fig. 3; 10-nH bonding wire is considered.

270 MHz. This UWB pulse generator provides high-data-rate transmission with low power consumption. Without the output buffer, the pulse generator achieves 2 pJ/pulse at 270 MHz f_p and 0.56 pJ/pulse at 90 MHz. If we use three pulses to represent 1 b, the circuit has the potential to reach a 90-Mb/s data rate. We should notice that in the circuit, while the pulse generator is compact, the power stage (buffer) is independent. This allows the designer to choose the desired power budget. In this transmitter, the power cost of the pulse generator can be considered to be negligible compared with the buffer stage. The tradeoff in power consumption and transmission distance can also be controlled by changing the amplitude of VCCB.

IV. WIRELESS TRANSMISSION TEST RESULTS

Fig. 9 is the S11 parameter Smith chart of the antenna measured by using a network analyzer and calculated in a 50- Ω system. We modeled the bonding wire as a 10-nH inductor and added a real inductor on the antenna to measure the S11 coefficient. We calculated the antenna efficiency, that is, the ratio of power delivered into the antenna and the maximum available power from the buffer. The antenna has a loss of 4–8 dB over the 350- to 1000-MHz range, as illustrated in Fig. 10. We also measured the received spectrum by using different Tx antennas. We tested the triangular onboard printed-circuit board (PCB) antenna, triangular copper antenna (the same with the receiver antenna), and 0.5-in. metal wire as a monopole antenna. The result is shown in Fig. 11. In this test, we place the receiver antenna 1 cm from the transmitter antenna and feed the received signal to the spectrum analyzer. The pulse rate is 270 MHz, modulated by 5-Mb/s random data. The onboard PCB antenna transmitted more energy than other antennas. While biocompatible antenna design is outside the scope of this work, it is an active research area to study [18]. More efficient antennas will be able to increase the transmission range.

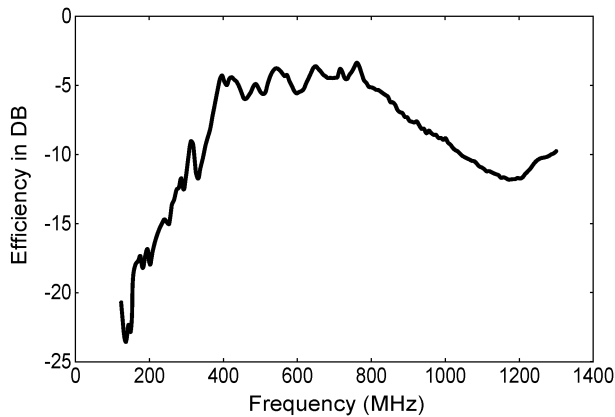


Fig. 10. Calculated transmission efficiency (power out over the maximum input power) of the antenna in Fig. 3. The calculation is based on a 50- Ω system with 10-nH parasitic inductance from the bonding wire. The mismatch is a loss of 4 to 8 dB over the 350- to 1000-MHz range.

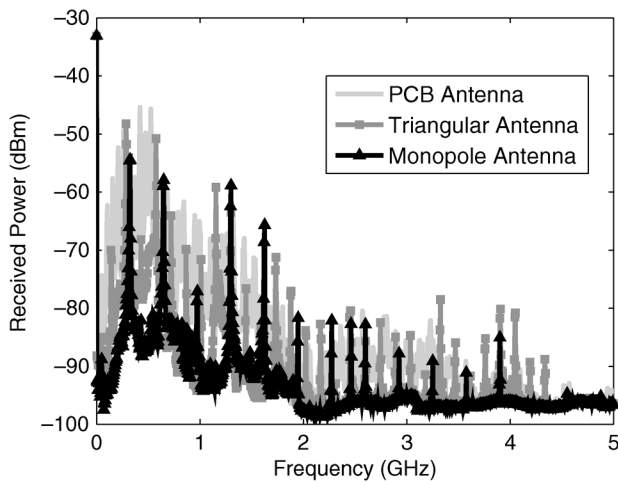


Fig. 11. Comparison of received spectrum from different Tx antennas. The triangular onboard PCB antenna transmitted more energy than other antennas.

We designed a UWB transmitter using the SOS pulse generator and used an OpalKelly 3001v2 FPGA board for operating and testing the pulse-based radio. The power supply and input signals can be provided by the FPGA. VCCB is used as a digital input to operate the transmitter in pulse amplitude modulation (PAM) mode (turning the pulse on and off, also known as ON/OFF keying or OOK) [1].

We used an Analog Devices' ADL5513 logarithmic RF detector as the receiver. The output of the device is a function of the input RF signal power. The minimum receiver output amplitude is 500 mV and this amplitude increases with higher RF input power. The receiver was designed to detect 1-MHz to 4-GHz RF power of -80 dBm or more. The response time of the evaluation board is 20 ns [19].

Fig. 12 shows the encoding of the signal with a pulse rate of 200 MHz. When VCCB (input signal) is high, the radio will send pulses to the transmitter antenna (radio output). The RF detector converts the pulses to the received waveform (detector output). The comparator digitizes the detector output into digital signals and sends them to the FPGA. The pulse amplitude is proportional to VCCB. In Fig. 12, the data rate is 14 Mb/s.

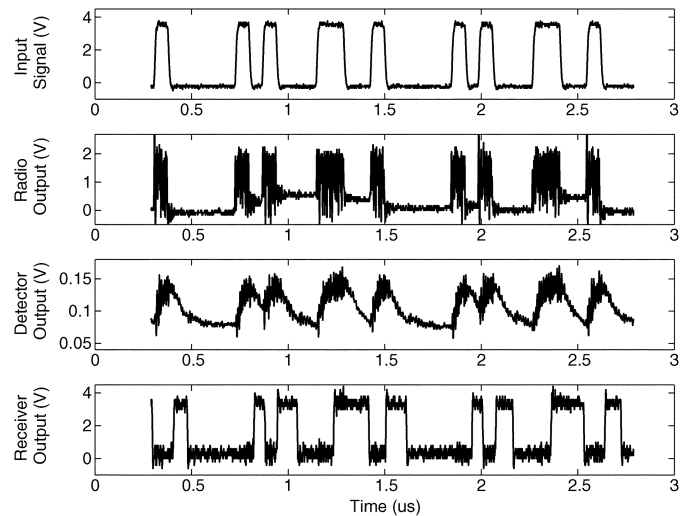


Fig. 12. Wireless communication test result at 14 Mb/s. The transmitter operates in ON/OFF keying mode with VCCB as the input. When VCCB (input signal) is high, the radio will send pulses to the transmitter antenna (radio output). The RF detector converts the pulses to the received waveform (detector output). The comparator digitizes the detector output to the digital signal and sends the data to the FPGA (receiver output).

The transmission distance is 40 cm. The data rate in the experiment is limited by the response time of the RF detector. In [20], a 5 Mb/s data rate is achieved with the RF detector AD8313 (Analog Device Inc.) with 40-ns response time. In this paper, we use the ADL5513 (Analog Devices, Inc.) with a 10-ns rising time and 20-ns falling time. A higher data rate (up to f_p) could be reached if a faster detector is available.

The transmission bit-error rate (BER) is also measured as shown in Fig. 14. Clock synchronization is performed by an all digital phase-locked loop (PLL) (ADPLL) implemented in the FPGA. The BER increases with the data rate and decreases with the transmission distance.

The transmitter works in an ON/OFF keying mode, with its power buffer sending pulses only when the data are "1." The transmitter power consumption is 21 mW with a data rate of 14 Mb/s, at a transmission distance of 4 m with 50% duty cycle data. In this case, the energy per bit is 1.5 nJ/b, which is 400 times more efficient than commercially available RF transmitters, such as Zigbee [21] (148.5 mW at 250 kb/s, 0.6 μ J/b), while providing a 56 times higher data rate. If we reduce the amplitude of the input signal, the power budget is able to reach 10 mW as shown in Fig. 13. If the transmission distance requirement is lower, we can further reduce the power by using a smaller-size transmitter output buffer, while maintaining the same data rate. This allows us to customize the design to specific implantable biosensors. The efficiency of the transmitter power can also be improved by using a high efficiency antenna, which is an area under active research [14].

The amplitude of the receiver output depends on the orientation and distance between the antennas. Fig. 15 shows the received power as a function of the distance between antennas when the VCCB is 3.3 V. The data in Fig. 15 are converted from the output amplitude to received power according to the ADL5513 data sheet. The sensitivity of the ADL5513 is -80

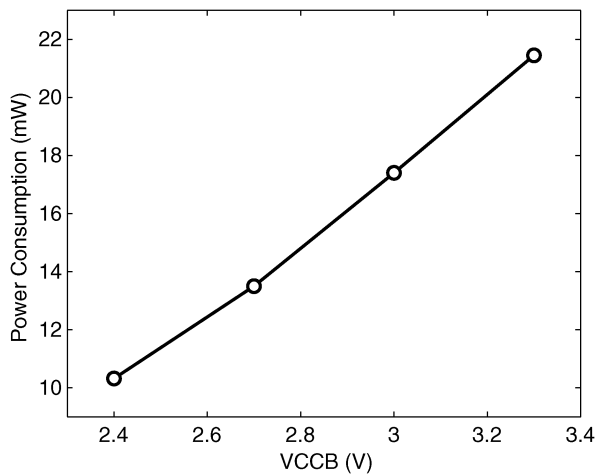


Fig. 13. Measured transmitter power consumption as a function of VCCB. The duty cycle of the input data is 50%.

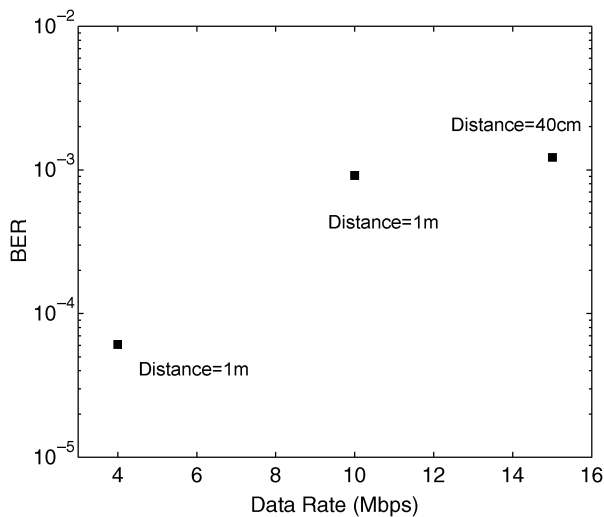


Fig. 14. Measured BER versus the data rate and transmission distance, using the Tx board antenna. The digital PLL is implemented in the FPGA for clock synchronization.

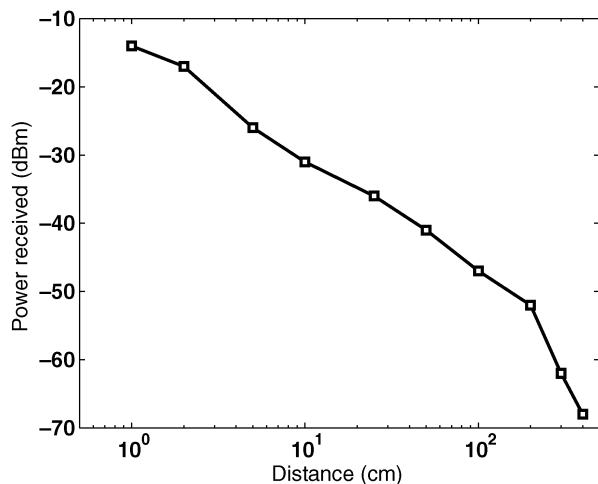


Fig. 15. Received power versus Tx and Rx distance. A commercial -80 -dBm wideband RF power detector can receive the signal from our UWB transmitter at up to 4-m distance.

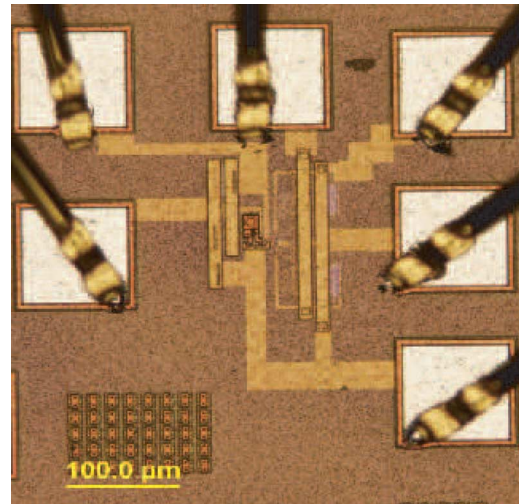


Fig. 16. Die micrograph of the integrated UWB pulse generator on a $0.5\text{-}\mu\text{m}$ silicon-on-sapphire CMOS process.

TABLE I
SUMMARY OF THE UWB PULSE-RADIO SYSTEM PERFORMANCE

Process Technology	SOS $0.5\ \mu\text{m}$ CMOS
Pulse Frequency f_p	90 MHz-270 MHz
Duration of Pulse	1 ns
Amplitude of Pulse	3.3 V
Pulse Generator Power Consumption	50 μW (at $f_p=90$ MHz) 0.6 mW (at $f_p=270$ MHz)
Pulse Generator Energy/pulse	0.56 pJ/pulse (at $f_p=90$ MHz) 2 pJ/pulse (at $f_p=270$ MHz)
Transmitter Power	10-21 mW (with 50% duty cycle data)
Transmission Distance (at -70 dBm received power)	4 m (21 mW power) 3.2 m (10 mW power)
Transmission Data Rate	14 Mbps
Transmission Energy/bit	1.5 nJ/bit
Chip Area (without pad)	$70\ \mu\text{m} \times 130\ \mu\text{m}$
Chip Area (with pad)	$420\ \mu\text{m} \times 420\ \mu\text{m}$
Antenna Size	2×1.5 inches
Antenna Efficiency	-4 to -8 dB
Antenna Bandwidth	350-1000 MHz

dBm. When the received power drops to -70 dBm, the transmission distance is 4 m when VCCB is 3.3 V. If VCCB is 2.4 V, the -70 -dBm distance decreases to 3.2 m. The transmitter and receiver antenna planes face each other, with the same height and orientation. Larger ranges can be attained with a more sensitive receiver.

V. SUMMARY

We designed, fabricated, and tested a silicon-on-sapphire low-power tunable UWB pulse generator which has the potential to be widely used in short-range low-power wireless biomedical applications. A micrograph of the IC is shown in Fig. 16. The test result shows that the transmitter circuit consumes 10–21 mW with a 14-Mb/s data rate. The core circuit occupies $70 \times 130\ \mu\text{m}$. Table I summarizes the main results and properties of the UWB transmitter circuit and system. Due to its low-power and high-speed performance, the circuit is a transformative technology candidate for high-data-rate and low-power wireless biomedical applications.

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Wei Tang (S'06) received the B.S. degree in electronics engineering from Peking University, Peking, China, in 2006 and is currently pursuing the Ph.D. degree at Yale University, New Haven, CT.

In 2007, he became a Research Assistant affiliated with Yale E-Lab. His research interests are analog/mixed-signal and low-power circuit design, wireless communication circuit design, and testing for biomedical applications.



Eugenio Culurciello (S'97–M'99) received the Ph.D. degree in electrical and computer engineering from Johns Hopkins University, Baltimore, MD, in 2004.

In 2004, he joined the Department of Electrical Engineering at Yale University, where he is currently an Associate Professor. He founded the E-Lab Laboratory at Yale University in 2004. His research interest is in analog and mixed-mode integrated circuits (ICs) for biomedical instrumentation, bio-inspired sensory systems and networks, biological sensors, and silicon-on-insulator design.