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Patch-clamp amplifiers on a chip

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ABSTRACT

We present the first, fully integrated, two-channel implementation of a patch-clamp measurement system. With this “PatchChip” two simultaneous whole-cell recordings can be obtained with rms noise of 8 pA in a 10 kHz bandwidth. The capacitance and series-resistance of the electrode can be compensated up to 10 pF and 100 MΩ respectively under computer control. Recordings of hERG and Na_v 1.7 currents demonstrate the system’s capabilities, which are on par with large, commercial patch-clamp instrumentation. By reducing patch-clamp amplifiers to a millimeter size micro-chip, this work paves the way to the realization of massively parallel, high-throughput patch-clamp systems for drug screening and ion-channel research. The PatchChip is implemented in a 0.5 μm silicon-on-sapphire process; its size is 3 × 3 mm^2 and the power consumption is 5 mW per channel with a 3.3 V power supply.

1. Introduction

The patch-clamp amplifier is a ubiquitous tool for characterizing ion-channel activity. For the screening of pharmaceutical compounds or the characterization of expressed channels, high-throughput patch-clamp systems are being developed, where recordings are made from cells in each well of a 96- or 384-well plate. In these systems the recording is made not with a glass pipette, but from a planar electrode at the bottom of each well (Fig. 1). An important part of such highly-parallel recording systems is a high-density array of patch-clamp amplifiers. We present here a highly miniaturized patch-clamp amplifier with complete whole-cell measurement capabilities.

Important constraints in building massively parallel patch-clamp systems have been the size and cost of the amplifiers, heat dissipation – which restricts the proximity of the amplifiers to the cells – and cross-talk between channels. The integrated “PatchChip” amplifier presented in this paper solves all of these design requirements, and is based on experience from our prototypes (Weerakoon et al., 2009, 2007a,b; Laiwalla et al., 2006a,b,c).

The dual-channel patch-clamp system occupies 3 × 3 mm^2 of area and consumes just 5 mW of power per channel. It is fabricated using a standard silicon-on-sapphire fabrication process, which allows parasitic capacitances and cross-talk effects to be minimized.

2. Materials and methods

Fig. 2 shows a block diagram of one channel of the PatchChip system. The two channels of the system are identical. The main signal path is from the electrode current I_{in} to the monitor voltage output $V_{out} = I_{in}R_f$, through operational amplifiers A1, A2, and A3.

Cells are stimulated by controlling the voltage $V_p = V_{clamp}$ at the electrode and measuring the resultant ionic current I_{in}. The goal of the compensation circuits is to allow step changes to be applied to the cell membrane potential V_m while the ionic current I_i is measured. The cell membrane can be modeled as a capacitance C_m in parallel with the membrane resistance R_m. The headstage of the patch-clamp recording system consists of a current-to-voltage transimpedance amplifier A1. The feedback resistor R_f is selectable in eight steps from 50 kΩ to 10 MΩ. Small shunt capacitors stabilize the feedback loop while yielding a bandwidth of a minimum of 300 kHz (with R_f = 10 MΩ) when the total capacitance on the input node is 30 pF. A difference amplifier A2 subtracts V_{clamp} from the transimpedance output. The resultant output voltage V_{out} is proportional to the input current, I_{in}.

The output filter A3 represents two poles of a three-pole, 20 kHz anti-aliasing filter. The third pole is presented by an external capac-

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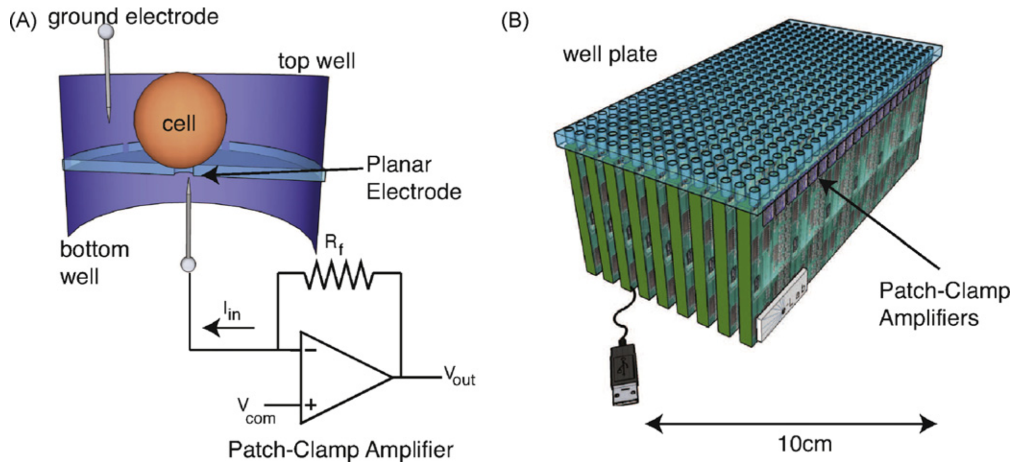

Fig. 1. (A) Patch-clamp amplifier performing whole-cell membrane current recording using a planar electrode. The planar electrode replaces the traditional glass micropipette with a micron sized-aperture that is topologically equivalent to the glass tip of the pipette. Cells are introduced into a well, and when suction is applied, the cells seal into the aperture. Further suction is applied to rupture the cell so that a whole-cell configuration is established. (B) Using the amplifiers presented in this paper, it is possible to design a high-throughput, automatic patch-clamp system that operates on entire 384-well plates. The wells on B are identical to the one in (A). Requirements for the amplifier are millimeter-size dimensions and minimized heat dissipation, cross-talk and low fabrication cost.

itor and is the only "glue" component required for the analog interface between the PatchChip and the external A–D converter. Similarly, the two-pole input reconstruction filter A6, critically damped with a time constant of 2 μs, smooths the input command signal V_{com} delivered directly from an external D–A converter and prevents rapid steps from causing nonlinearities and slew-limiting in the other amplifiers of the system.

2.1. Electrode compensation circuitry

The system compensates for the difference between the actual membrane voltage V_m and the clamping voltage V_{clamp} due to the voltage drop across the pipette electrode series resistance R_s. The circuit also compensates for the current i_{prs} drawn by the electrode parasitic capacitance C_{prs} and by the seal leakage-resistance R_L. R_s

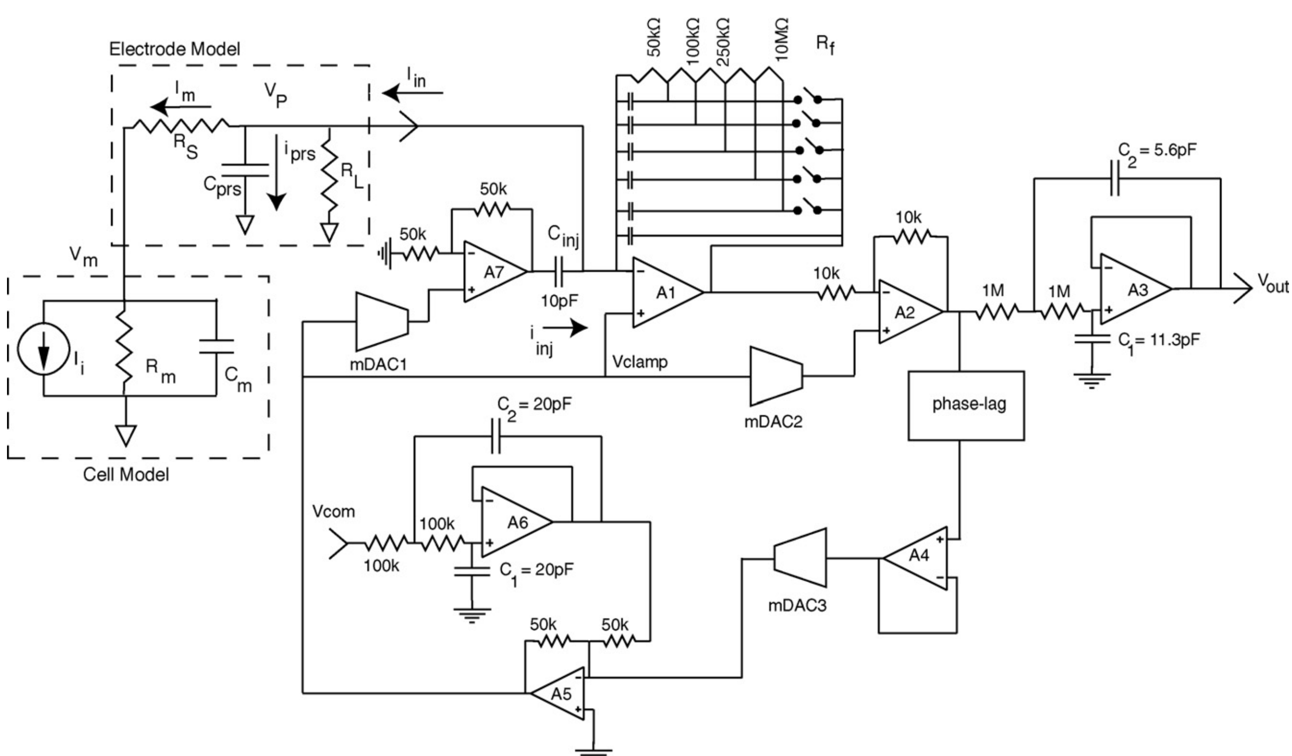

Fig. 2. One channel of the two-channel integrated patch-clamp system and the electrical model of a cell and pipette electrode. The main signal path is from the electrode current I_{in} to the monitor voltage output $V_{out} = I_{in}R_f$, through operational amplifiers A1, A2 and A3. Multiplying digital to analog converter mDAC1 controls the parasitic capacitive compensation, mDAC2 provides leak subtraction, mDAC3 and the phase-lag controller circuit provides series resistance compensation. Input reconstruction and output anti-aliasing filters are also integrated. mDAC1 and mDAC2 are voltage-mode, R-2R DACs with $R = 50\,k\Omega$, minimum gains of 0.5, and resolutions of 8 and 10 bits, respectively. mDAC3 is a 9-bit hybrid transconductance-mode DAC with a maximum transconductance of 0.2 mS. Typical values of the electrode and cell elements are C_{prs} =5 pF, R_L = 100 MΩ, R_s = 10 MΩ, C_m = 30 pF, R_m = 100 MΩ and peak values of I_i are 1–10 nA.

compensation is necessary for two reasons. First, it allows accurate voltage clamping of the membrane by reducing the errors from the voltage drop across the series access resistance R_s. Second, the compensation reduces the time needed to charge C_m enabling the circuit to monitor ion-channel events occurring immediately after changes in V_{com} is applied (Sigworth, 1995b). The drop across R_s is predicted by adding a fraction of V_{out} to the applied membrane-command potential V_{com} by means of amplifier A5, to obtain V_{clamp}. The fraction of compensated series-resistance is determined by the 9-bit mDAC3, which at full-scale yields compensation for a resistance of $10 \times R_f$. mDAC3 was designed as a hybrid weighted-resistor and R-2R device to minimize the noise gain of the A5 stage. A passive phase-lag compensation circuit is included in the positive-feedback loop if desired, to improve stability when a high percentage of R_s, e.g. more than 90%, is compensated.

For effective R_s compensation the measured current must be equal to the current I_m flowing through R_s. The charging current of the parasitic electrode capacitance C_{prs} and the current through the leakage conductance R_L therefore must first be subtracted from the measurement of I_{in}. The capacitive-current subtraction is done by injecting a current i_{inj} through an integrated capacitor C_{inj} of 10 pF. The gain α_{inj} of the amplifier A7 is determined by the 8-bit mDAC1 to be between 1 and 2. The compensated capacitance is equal to $(\alpha_{inj} - 1)C_{inj}$.

The differential amplifier A2 is unbalanced when the voltage-output mDAC2 is set to a gain different from its minimum value of 0.5. As its gain increases, subtraction is provided for the excess I_{in} on the input. The maximum gain of the 10-bit mDAC2 is unity, allowing for compensation of a leakage resistance as high as R_f. All three compensation circuits are controlled using a serial digital control bus. A 64-bit shift register and buffer register store the bit patterns for the mDACs and various switches in one patch-clamp channel.

2.2. Voltage swings and R_f

Modern patch-clamp amplifiers contain an additional "C-Slow" compensation circuit to remove the large current transients due to the charging of the membrane capacitance C_m, which is typically in the range of 20–40 pF. These circuits have been implemented as a first-order state-variable filter (Sigworth, 1995a,b) in which the time constant is roughly 100 μs to 1 ms. Due to the limited capacitor sizes, and therefore short time constants, that can be realized in a monolithic circuit, we decided not to provide this "slow capacitance" compensation. Instead, this compensation will be provided in software. We rely on the use of a 16-bit or higher resolution A–D converter to digitize the current–monitor signal V_{out} so that the large charging transients can be subtracted digitally.

In the absence of slow-capacitance compensation, the entire charging current of the membrane capacitance must be injected through the feedback resistor R_f. Thus the voltage swing available at the output of amplifier A1 becomes an important issue. We have used a 3.3 V silicon-on-sapphire (SOS) process, so that the analog power-supply voltages are ±1.6 V. Although the typical membrane-potential excursions are only in the range ±150 mV, when R_s compensation is in use the excursions of V_p can be an order of magnitude larger.

Consider the case in which a fraction k of the series resistance is compensated. When a voltage step of magnitude ΔV_{com} is applied to V_{com} the effect of the R_s compensation feedback is to produce an initial step $\Delta V_p = \Delta V_{com} / (1 - k)$. For example, a 150 mV step with $k = 0.8$ (80% compensation) yields an initial step of 750 mV. Even ignoring the current through R_L the initial current will be $I_{in} = \Delta V_p / R_s$ and will have to be sourced through the feedback resistor R_f. Thus the initial voltage at the output of A1 ($V_{out,A1}$) will need to be

$$V_{out,\mathrm{A1}} = \frac{\Delta V_{com}(R_s + R_f)}{(1 - k)R_s} \quad (1)$$

If R_f is chosen to be equal to R_s in this example, the initial value of $V_{out,A1}$ must be 1.5 V, very close to the available supply voltage of 1.6 V. To avoid amplifier saturation therefore, two steps must be taken. First, R_f must be kept to a low value, typically 5–10 MΩ in cases where R_s is in this resistance range. Second, amplifier A1 (and also other amplifiers in the circuit) must have a rail-to-rail output swing capability. The characteristics of the operational amplifiers are described in Section 2.4.

The low value of the feedback resistor R_f means that the current–monitor signal of the PatchChip will have a substantial contribution from the resistor's thermal noise; in a 10 kHz bandwidth this noise is 4 pA rms when $R_f = 10$ MΩ. The thermal noise arising in R_s is also large, and when its value is equal to R_f, its noise is equal to that from R_f at high frequencies $f > f_c$, where $f_c = 1/(2\pi R_s C_m)$. When R_s compensation is in use, which in effect increases the recording bandwidth beyond f_c, the two resistances R_f and R_s make nearly equal contributions to the noise variance. Thus the low value of R_f does result in increased noise, but the increase is moderate, about a factor of $\sqrt{2}$ over the theoretical minimum noise due to R_s alone.

2.3. Silicon-on-sapphire technology

The PatchChip was implemented using the silicon-on-sapphire (SOS) technology. SOS offers several advantages over conventional bulk CMOS technology, as is illustrated in Fig. 3. First, the absence of a conducting substrate greatly reduces parasitic capacitance and allows the fabrication of large, nearly ideal resistors. In conventional bulk-CMOS processes the source and drain of each transistor is isolated from the substrate by a reverse-biased diode; these diodes contribute a considerable capacitance to each such node in

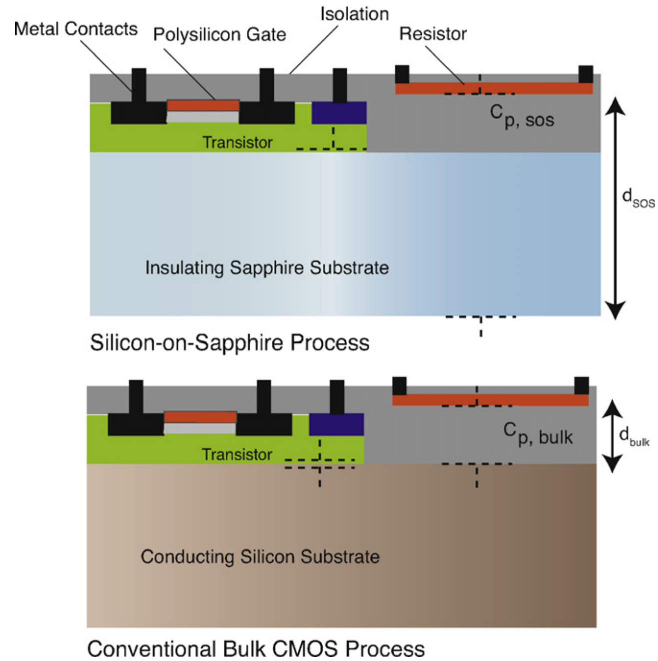

Fig. 3. The patch-clamp system was implemented using silicon-on-sapphire (SOS) technology. The insulating substrate in SOS (top) reduces parasitic capacitance and allows fabrication of large resistors to implement R_f with no degradation in frequency response. The insulating substrate reduces cross-talk between channels and allows devices to operate at faster speeds than conventional bulk CMOS technology (bottom).

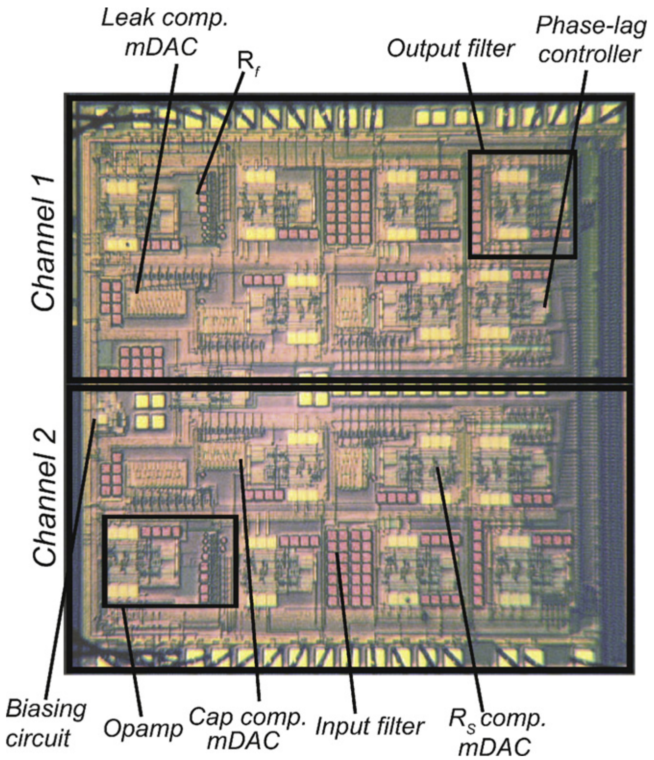

Fig. 4. A micrograph of the test circuit in silicon-on-sapphire technology. The fabricated die contained two channels and occupied just 3 × 3 mm^2. Each channel has series resistance, parasitic capacitance and leak compensation capability. After initial setup expenditures, each amplifier costs just a few dollars to manufacture.

the circuit. Even resistor elements, which are isolated from the bulk silicon by oxide layers, show considerable parasitic capacitance because the oxide layers are relatively thin. In SOS on the other hand, transistors and resistors are fabricated on top of the thick sapphire substrate (Fig. 3) and therefore experience vastly smaller parasitic capacitances (Culurciello et al., 2007). Second, the non-conducting substrate provides a better means of isolating devices on the substrate, yielding better cross-talk performance between patch-clamp channels. Third, the insulating substrate allows the power supplies for digital and analog parts of this mixed-signal circuit to be separated to obtain better noise performance. Fourth, the lower parasitic capacitance allows SOS devices to perform at faster speeds and lower power than those made using conventional bulk CMOS technology (Culurciello, 2010). The final layout of the microchip implementing the two-channel patch-clamp system is shown in Fig. 4. This layout is the physical implementation of the circuits reported in Fig. 2.

2.4. High-performance operational amplifier design

A low-noise, rail-to-rail, constant-transconductance operational amplifier was designed specifically for this system (Weerakoon et al., 2010). SOS transistors have low output resistance and therefore yield low voltage gains; we therefore made extensive use of cascode circuits, obtaining with this three-stage design a DC gain of 75 db and a gain-bandwidth product of 12 MHz for unity-gain operation. Fig. 5 shows the fabricated operational amplifier, which occupies an area of less than 0.1 mm^2. Rail-to-rail operation of the amplifier is needed to maximize voltage swings with the small power-supply voltages. The amplifier reported a 3 nV/$\sqrt{\text{Hz}}$ of input-referred voltage noise in a bandwidth of 10 kHz, and <1 mV of input-referred offset, while consuming 1.4 mW of power. Table 1 reports a summary of the amplifier characteristics.

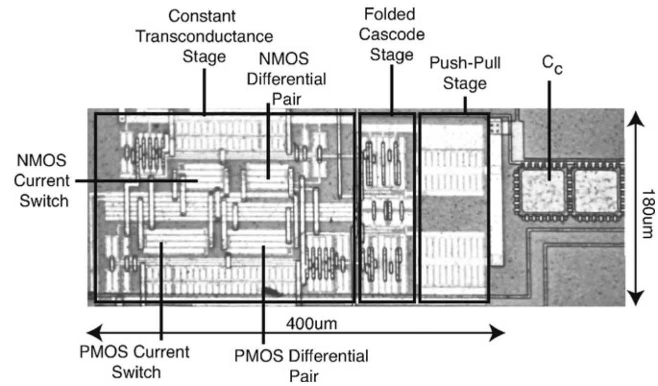

Fig. 5. A die micrograph of the fabricated operational amplifier. The operational amplifier occupies an area of 0.08 mm^2 providing rail-to-rail output voltage and constant gain-bandwidth product over the entire rail-to-rail common-mode range. The capacitor C_c is the frequency-compensation capacitor.

3. Results

We have extensively tested the electrical properties of the two-channel patch-clamp system, and its functionality in patch-clamp recordings from cells. In these tests the system was controlled and data were acquired using the JClamp patch-clamp software (www.scisoftco.com). The results are comparable to those from commercial non-integrated patch clamp amplifiers.

Fig. 6 shows the measured step responses of the series resistance compensation circuit. The time constant τ associated with charging the membrane capacitance C_m through a compensated resistance ($R_S - R_{comp}$) when a step V_{com} is applied (inset), is given by $\tau = C_m(R_S - R_{comp})$. Increasing compensation, R_{comp} approaches R_S and τ decreases, increasing recording bandwidth. Using the series resistance compensation circuit, we compensated 3–4 MΩ of the 4 MΩ electrode series resistance, decreasing the time needed to charge C_m from τ = 200 to 50 μs (75% compensation) and about 120 μs (100% compensation). Full resistance compensation can only be obtained with the phase-lag compensation circuit, which yields complete compensation at low frequencies but slows the settling time of the system.

Fig. 6 shows the measured step response of the electrode capacitive compensation circuit. When uncompensated, the headstage provides the current i_{prs} needed to charge the parasitic capacitance. This current appears as spikes in the current–monitor signal with the same polarity as V_{com}. When properly compensated, the spikes are greatly reduced in size.

Fig. 7 shows measured simultaneous data from both channels of the system. We applied a large voltage step (100 mV) to one channel with a model cell connected to its input terminal. The cross-talk on the adjacent non-measuring channel is 40 dB lower even with 80% series resistance compensation in use.

Table 1
Measurement results for the operational amplifier designed for the patch-clamp system. A load resistance of 15 kΩ and a 3.3 V power supply was used in the measurements. The operational amplifier met all design specifications.

Die area	0.08 mm^2
Open loop gain	75 dB
Gain-bandwidth product	12 MHz
Input-referred offset voltage	0.4 mV
Input common-mode range	0–3.3 V
Output swing	0–3.3 V
Slew rate	10 V/μs
Input-referred voltage noise at 10 kHz	3×10^{-9} V/$\sqrt{\text{Hz}}$
Quiescent current	430 μA
Input capacitance	2.6 pF

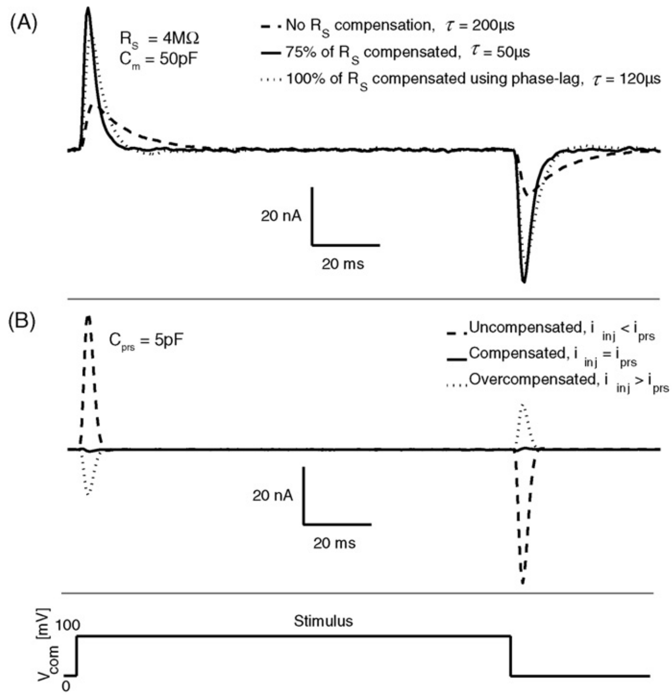

Fig. 6. (A) Measured response of the series resistance compensation circuit when compensating a 4 MΩ electrode series resistance. The time needed to charge C_m was reduced from $\tau = 200$ to 50 µs (75% compensation) and 120 µs (100% compensation with phase-lag). (B) Measured step response of the electrode capacitive compensation circuit when compensating 5 pF at the input. When uncompensated, the headstage provides the current i_{prs} needed to charge the parasitic capacitance. This current appears as spikes in the current–monitor signal. When properly compensated, $i_{prs} = i_{inj}$ and the spikes do not appear. When overcompensated, $i_{inj} > i_{prs}$ and the spikes reverse polarity.

Fig. 8 shows a whole-cell recording from an HEK293 cell expressing hERG channels. We compensated the 6.5 pF parasitic capacitance, and 80% of the 4.2 MΩ series resistance present at the input. R_f was set to 5 MΩ. The peak tail current curve in (C) shows the standard voltage dependence of inactivation and activation in the channels.

Sodium-channel currents present a particularly demanding test for a whole-cell recording system. The rapid kinetics and negative-resistance characteristic of these currents requires good R_s compensation. Fig. 9 shows single-sweep recordings from an

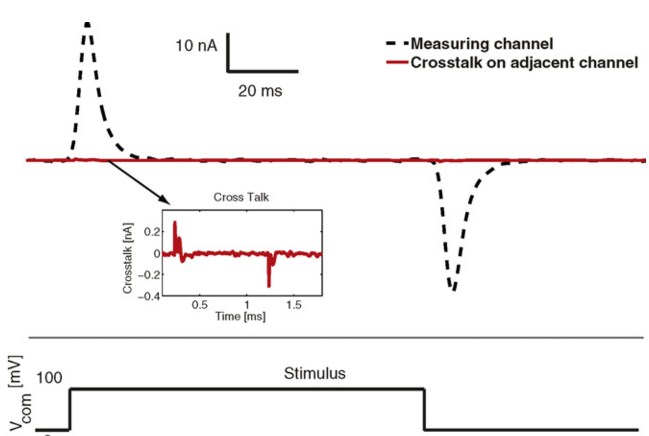

Fig. 7. Measured cross-talk between channels. A voltage step of 100 mV was applied to one channel, which was driving a model circuit with 80% series-resistance compensation. The current–monitor signal in the adjacent non-measuring channel is at least 40 dB lower.

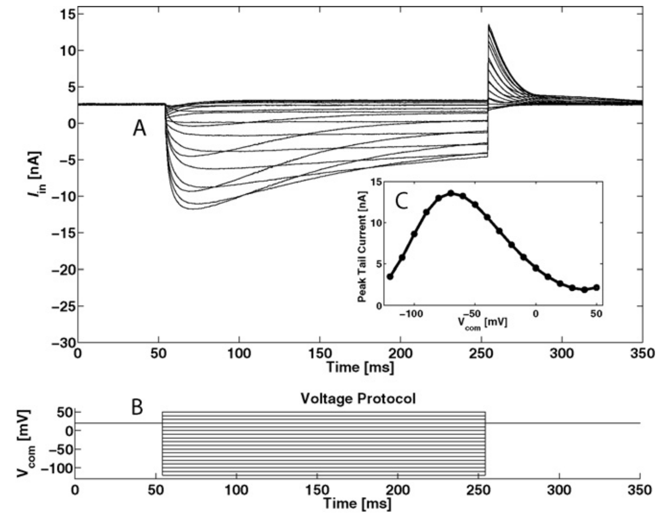

Fig. 8. (A) Single-sweep responses from an HEK 293 cell expressing hERG channels. R_s was 4.2 MΩ of which 80% was compensated. C_{prs} of 6.5 pF was fully compensated. C_m was 40 pF. (B) The cells were held at 20 mV and stepped to potentials of −130 mV to 50 mV in 10 mV increments for 200 ms. (C) The tail currents at +20 mV are plotted vs. V_{com} from A. The extracellular solution contained (mM) 117 NaCl, 13 KCl, 10 HEPES, and 5 EGTA. The pipette solution contained 160 KCl, 1 EGTA, and 10 HEPES. Currents were sampled at 100 kHz and filtered at 10 kHz.

HEK293 cell expressing Na_v 1.7 channels. Linear leak and residual capacitance artifacts were subtracted using the $-P/6$ method. This protocol (using six inverted pulse sequences scaled down by a factor of 6, delivered at negative membrane potentials) increases the net rms noise in the traces about threefold. Despite the large cell capacitance ($C_m = 40$ pF) the clamp time constant was 40 µs, giving a faithful current time course. The peak current–voltage curve (Fig. 9) shows steep activation of the channel currents with no evidence of series-resistance error (Estacion et al., 2008).

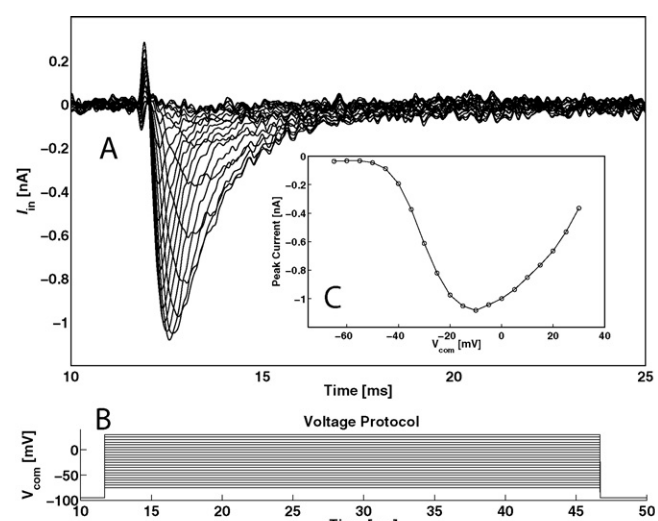

Fig. 9. (A) Single-sweep responses of HEK 293 cells expressing Na_v 1.7 sodium channels, after linear leak subtraction using the $-P/6$ protocol. The leak subtraction increases the net rms noise in the traces about threefold. R_S was 4.5 MΩ of which 80% was compensated. C_{prs} of 7 pF was fully compensated. C_m was 40 pF. (B) To generate activation curves, the cells were held at −100 mV and stepped to potentials of −75 to 30 mV in 5 mV increments for 35 ms. (C) The peak currents vs. V_{com} from (A). The current–monitor signal was filtered at 10 kHz and sampled at a 100 kHz rate. The recording was made at room temperature. The extracellular solution contained (in mM) 127 NaCl, 13 KCl, and 10 HEPES. The pipette solution contained 10 NaCl, 140 CsF, 10 HEPES, and 1 EGTA.

Table 2
Key features of the two-channel patch-clamp system.

Technology	0.5 μm silicon-on-sapphire
Number of channels	2 per die
Silicon area	$3 \times 3\,mm^2$ per die $1.5 \times 3\,mm^2$ per channel
Power consumption	5 mW per channel at 3.3 V
Capacitive compensation	10 pF max
Series resistance compensation	80% up to $10 \times R_f$, or 100% with phase-lag compensation
Leak compensation	Conductance up to $1/R_f$
Current noise	8 pA rms input-referred in a 10 kHz bandwidth ($R_f = 10\,M\Omega$)
Variable feedback resistor R_f	50, 100, 250, 500 kΩ 1, 2.5, 5, 10 MΩ
Dynamic range	± 20 μA
Reconstruction filter	2 poles, 60 kHz cutoff
Anti-aliasing filter	3 poles, 20 kHz cutoff
Nonlinearity	<0.1%
Cross-talk between adjacent channels	−40 dB (at 80% series resistance channels compensation)

Table 2 summarizes the key features of the PatchChip. The two-channel system occupies $3 \times 3\,mm^2$ of area and consumes 5 mW of power per channel. The low power consumption allows the amplifiers to be placed in close proximity to the cells under test. The input-referred noise is 8 pA rms at 10 kHz bandwidth.

4. Discussion

We have implemented a two-channel patch-clamp system in silicon-on-sapphire on a $3 \times 3\,mm^2$ chip area. The system reports below −40 dB of cross-talk between adjacent channels and the input-referred current noise of the system is 8 pA rms in a 10 kHz bandwidth. The appropriate setting of the feedback resistor, 5–10 MΩ for typical whole-cell recordings, means that the resistor's thermal noise makes a contribution; however this contribution is moderate in comparison to the thermal noise from the series resistance of the electrode-and-cell combination. The system is able to compensate series resistances and parasitic capacitances up to 100 MΩ and 10 pF respectively. The power consumption of the device is 5 mW per channel at 3.3 V. This accurate, low-noise system with electrode compensation can replace a commercial rack-mounted patch-clamp system; more importantly it can also be integrated into a massively parallel, high-throughput, patch-clamp system that can significantly advance the state-of-the-art in drug screening and ion-channel research.

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