Three-dimensional phototransistors in 3D silicon-on-insulator technology

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Measurement results of phototransistors designed in a three-dimensional (3D) 0.18 μm silicon-on-insulator technology are presented. The phototransistors respond to light intensities of 5–200 000 lux with currents from 50 fA to 2.3 μA. The novelty of this phototransistor is that its photocurrent is proportional to the square of the incident light intensity. The device measurements reported show that the photodetectors can be used for the design of high-density imaging arrays in three-dimensional SOI CMOS fabrication processes.

Introduction: Three-dimensional integrated-circuit technologies promise to offer integrative advantages in the vertical dimension for stacking both homogenous and heterogeneous layers of conventional CMOS dies [1, 2]. Recently heterogeneous imaging sensor arrays have been presented with one million vertical connections between dies [3]. This array was obtained by wafer stacking a 0.35 μm silicon-on-insulator (SOI) CMOS on top of 0.35 μm bulk CMOS used to obtain photosensitive elements. The bottom layer die was thinned to allow back-light illumination to reach the detectors, and mounted on a glass substrate for mechanical stabilisation. The main reason for the use of bulk CMOS was the unavailability of photodetectors in SOI CMOS.

This Letter presents the design and measurements obtained from native SOI phototransistors fabricated in the first available three-dimensional (3D) multiproject run offered by MIT Lincoln Laboratories. A cross-section of the Lincoln Labs 3D die stack is shown in Fig. 1. Two thinned SOI dies (tiers 2 and 3) are stacked upside-down on top of another die (tier 1). Vertical interconnects are obtained by means of a low-temperature metallisation process. The contribution of this Letter is to: (i) present phototransistors obtained with native rules on the 3D SOI process, and (ii) show that these SOI devices respond to light with a quadratic relationship, and with a sensitivity higher than linear SOI photodetectors obtained in the same process. Our device will allow the use of a standard SOI layer as photodetector layer for vertically integrated image sensor arrays. This device eliminates the need of heterogeneous integration of bulk CMOS dies and the need for die-thinning techniques to image light.

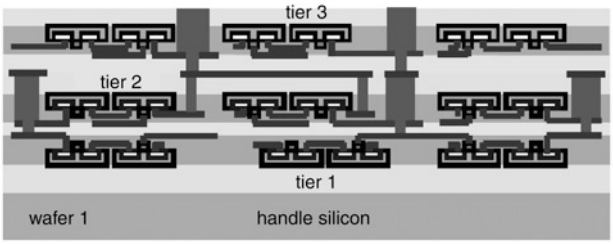

Fig. 1 *Cross-section of MIT Lincoln Laboratories three-dimensional integration of three SOI dies*
Detectors implemented in tier 3

Photosensitive devices: We report here on the results obtained by a phototransistor obtained in the 3D process. The NMOS phototransistor has an octagonal layout, as shown in Fig. 2, where source and drain diffusions are separated by a floating polysilicon (poly) gate. We implemented the phototransistor in the top SOI layer (tier 3). The silicon layer is 50 nm thick. While we have no control over process parameters as layers thickness and organisation, we have designed and optimised the detectors for maximum dynamic range, taking advantage of the process specifications. To maximise the dynamic range, we took particular care in the layout to avoid possible causes of leakage currents at the diode junction. The layout of the detector is circular, to avoid interfaces between the source and drain *n*-diffusions and the deposited local oxidation of silicon (LOCOS). For the same reason, the phototransistor has been gated with a polycrystalline silicon layer to avoid having low-quality silicon oxide deposited above its channel. The poly layer ensures a low-leakage thermally grown oxide layer and thus prevents the interface currents that plagued previous SOI photodetectors [4, 5]. The phototransistor gate was left floating. We have not tested devices with the gate connected to source, so we cannot comment on this detector topology. *p*-type phototransistors and all other photodetectors without the channel doping layer (CBN/CBP) did not provide any photosensitivity. The channel doping layer is of 5×10^{17} atoms/cm^3.

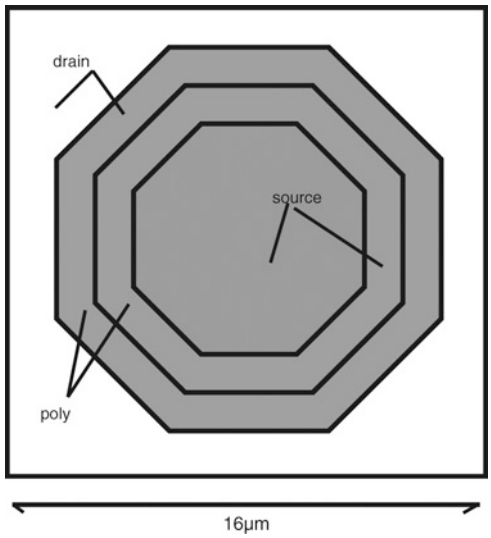

Fig. 2 *Octagonal layout of fabricated phototransistor*
Source and drain diffusion separated by polysilicon gate

Results and measurements: Photocurrent data (I_{ph}) was collected with a picoammeter unit. We used a conventional halogen light as a source (I_{in}), since the final application is the use of this sensor for indoor lighting. The light meter was a commercial photographic unit with a range of 1–20 000 lux. We used neutral density filters to measure high light intensities. Also, 1.5 V is the nominal supply voltage rating of the 3D process. Fig. 3 shows the responsivity of the 3D phototransistor when biased at 0.5 and 1 V. Note that the photocurrent almost reaches the saturation current for this device (2.36 μA) at 200 000 lux with 1 V bias. We computed a photocurrent model as in (1) and (2). The phototransistor did not provide light-sensitivity when biased at 1.5 V possibly because of depletion-region punch-through:

$$I_{ph}(0.5\,\mathrm{V}) = I_{in}^2 \times 1.7 \times 10^{-16} \quad (1)$$

$$I_{ph}(1\,\mathrm{V}) = I_{in}^2 \times 2 \times 10^{-17} \quad (2)$$

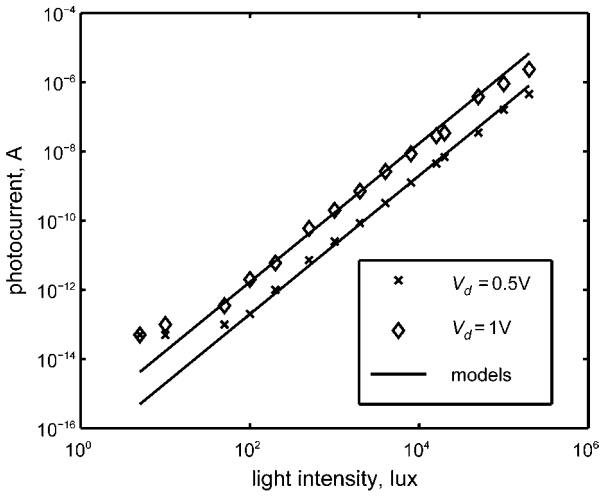

Fig. 3 *Responsivity of MOS top-layer phototransistor against bias voltage*
Photocurrent model is proportional to square of incident light power

In this MOS structure the photocurrent is proportional to the square of the incident light power. This power law is due to two combined effects: (i) the light-induced generation of carriers in the fully-depleted device body (I_{ph1}), and (ii) the resilience of majority carriers in the device body

[6] modulating the transistor threshold voltage (I_{ph2}). The parasitic bipolar transistor in parallel with the NMOS is responsible for the photogenerated current, as expressed in (3). The body of the transistor is floating in SOI. Holes and electrons are generated by the incident light in the transistor body:

$$I_{ph} = I_{ph1} I_{ph2} \tag{3}$$

I_{ph1} is the photocurrent generated by the depleted body by the incident light, and can be expressed as $I_{ph1} = k_1 I_{in}$, where k_1 is a bias- and process-dependent constant. On the other hand, I_{ph2} can be expressed by (4), where V_{th} is the thermal voltage, k_2 is a bias- and process-dependent constant, and V_{bs} is the transistor body-to-source voltage:

$$I_{ph2} = k_2 e^{V_{bs}/V_{th}} \tag{4}$$

The electrons are quickly swept from the NMOS channel to the drain, while majority carriers are trapped in the body [6]. These majority carriers modulate the body-to-source voltage V_{bs} with the relation expressed in (5), and I_0 is the minimum detectable light giving rise to the dark current [7]:

$$V_{bs} = V_{th} \log \frac{I_{in}}{I_0} \tag{5}$$

By merging (3) with (4), we obtain (6), which explains the quadratic relationship between the light intensity and the photocurrent in the SOI NMOS phototransistors:

$$I_{ph} - \frac{k_1 k_2}{I_0} I_{in}^2 \tag{6}$$

The values of k_1 and k_2 can be established from the responsivity of a single photodiode in the process, with a value of 1.7×10^{-15} A. I_0 is the intensity corresponding to leakage current (1 fA) and its value was extracted to be 1 lux. Therefore the product $k_1 k_2$ will be 2×10^{-17} A at a 1 V bias voltage.

Conclusions: We have designed and measured photodetector devices with quadratic responses in a 3D SOI process. The NMOS phototransistors respond to light intensities of 5–200 000 lux with currents from 50 fA to 2.3 μA. The data in this Letter is essential to the design of imaging arrays in 3D SOI processes.

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