

Integrated patch-clamp biosensor for high-density screening of cell conductance

P. Weerakoon, F. Sigworth and E. Culurciello

The first fully integrated implementation of a patch-clamp measurement system is presented. The system was implemented in a 0.5 μm silicon-on-sapphire process. The system can record cell membrane currents up to ± 20 nA, with an rms noise of 5 pA at 10 kHz bandwidth. The system can compensate for the capacitance and resistance of the pipette electrode, up to 20 pF and 4 M Ω , respectively. The die size is 1150 by 700 μm . The power consumption is 3.3 mW at 3.3 V.

Introduction: The patch-clamp is the gold standard in electrophysiology and is a fundamental technique to screen drugs and medical compounds, and ultimately to ensure consumer safety [1]. The patch-clamp technique reports the highest signal-to-noise ratios available in a biosensor, but is labour-intensive when performed manually [2]. We present a silicon-on-sapphire integrated patch-clamp measurement system, an enabling technology to perform simultaneous and automatic measurements on a large number of cells in parallel. The fabricated device is a fully integrated system in less than 1×1 mm silicon area and 10 million times smaller in volume than commercial bench-top systems. The device will be used with planar patch-clamp electrodes [3–5] to implement the system portrayed in Fig. 1. This system employs four patch-clamp amplifier circuits per well to produce concurrent measurements from up to 1536 cells in less than a minute protocol time.

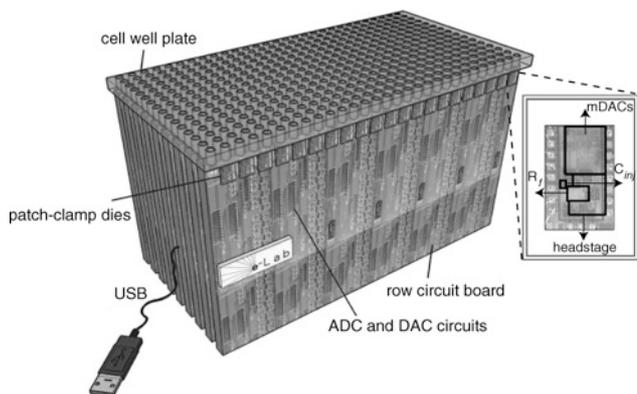


Fig. 1 High-density parallel patch-clamp system and micrograph of die

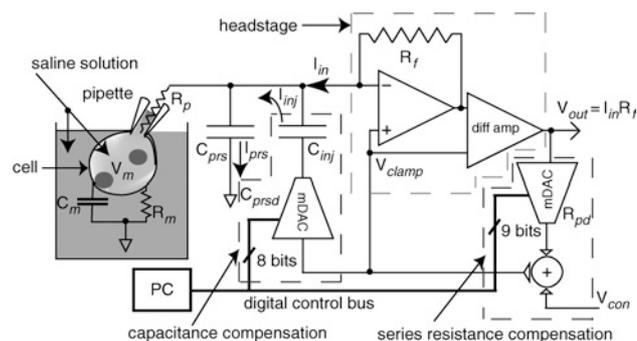


Fig. 2 Block diagram of integrated patch-clamp recording system with electrode compensation

Patch-clamp system overview: Fig. 2 shows a block diagram of the patch-clamp headstage and electrode compensation circuitry. Cells are stimulated by applying voltage steps across the cell membrane (V_{clamp}). The circuit then measures the resultant membrane current I_{in} in a range of ± 1 –20 nA. In whole-cell patch recording, a pipette filled with a saline solution is used to adhere to the cell. The cell membrane can be modelled as a capacitance C_m in parallel with the membrane resistance R_m . The system compensates for the difference between the actual membrane voltage V_m and the clamping voltage V_{clamp} due to the voltage drop across the pipette electrode series resistance R_p . The circuit also compensates for the current I_{prs} drawn by the electrode parasitic capacitance C_{prs} . The headstage of the patch-clamp

recording system consists of a current-to-voltage transimpedance amplifier that uses resistive feedback (R_f). A difference amplifier subtracts V_{clamp} from the transimpedance output. The resultant output voltage V_{out} is proportional to the input current, I_{in} .

Electrode compensation circuits: The drop across the series resistance of the pipette electrode R_p is compensated by feeding back a fraction of the current-monitoring signal to the control membrane potential V_{con} in positive polarity, to obtain V_{clamp} . A 9-bit digital setting R_{psd} of the compensated resistance is applied to a multiplying digital to analogue converter (mDAC) to control the amount of compensation. Series resistance compensation allows accurate voltage clamping of the membrane. The technique also reduces the time needed to charge C_m and enables the circuit to monitor ion-channel events occurring immediately after the control voltage is applied.

The parasitic electrode capacitance C_{prs} is compensated by injecting a current I_{inj} through an integrated capacitor C_{inj} of 5 pF. The device can compensate for parasitic capacitances up to 20 pF. An 8-bit digital setting of C_{prsd} is applied to an mDAC to control the amount of compensation. Parasitic capacitance compensation prevents the electronics from saturating since it eliminates capacitive overshoots. Furthermore, these fast currents can cause oscillations in the positive feedback loop of the resistive compensation and thereby in V_{clamp} . These oscillations can cause irreversible damage to the cells under test.

Experimental results: Fig. 3 shows the predicted and measured step responses of the electrode compensation circuitry. The left panel shows the effects of series resistance compensation. The time constant t_c associated with charging the membrane capacitance C_m through the compensated resistance ($R_p - R_{psd}$) is given by $t_c = (R_p - R_{psd}) C_m$. Therefore, when compensated, R_{psd} approaches R_p and t_c decreases. By compensating R_p , owing to charge conservation, t_c will decrease and the overshoot will increase. Using the series resistance compensation circuit, we were able to compensate for a 4 M Ω series resistance, decreasing the time needed to charge C_m from $t_c = 600$ μs to $t_c = 200$ μs . The right hand panel of Fig. 3 shows the predicted and measured response of the parasitic capacitance compensation circuit. When uncompensated, the headstage provides the currents needed to charge the parasitic capacitance. These currents appear as overshoots in the current monitoring signal with the same polarity as the control step. When properly compensated, $I_{prs} = I_{inj}$ and the overshoots do not appear. When overcompensated, $I_{inj} > I_{prs}$ and the overshoots appear negative.

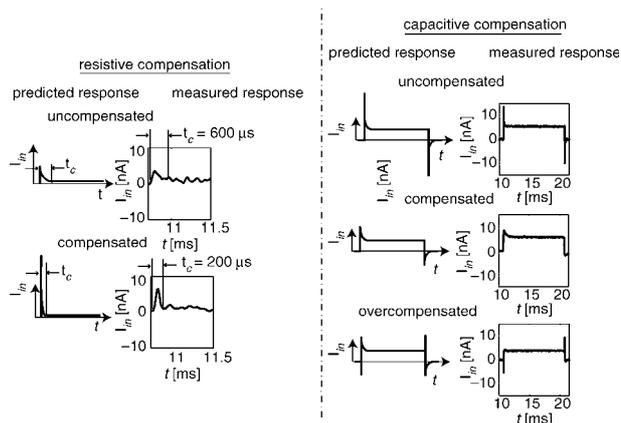


Fig. 3 Predicted and measured response of electrode compensation circuits

Fig. 4 shows the low-noise operational amplifier used in the headstage (top-left) and its measured characteristics (top-right). Low-noise amplification is critical to our design owing to the low amplitudes of the membrane currents. The current noise of the headstage can be shown to be inversely proportional to R_f . However, the physical size of R_f in layout and the headroom of the transimpedance amplifier limits the maximum achievable value. A value of 25 M Ω was chosen for our design. As seen from the graph to the bottom right of Fig. 4, the input referred current noise of the headstage is no greater than the noise contributed by the pipette electrode plus cell network. Integrating the input-referred noise yields an rms current noise of 5 pA at 10 kHz bandwidth. This corresponds to a signal-to-noise ratio of 250 or approximately 8 bits

in whole-cell patch-clamp measurements. This result is comparable to state-of-the-art commercially available bench-top amplifiers; e.g. the latest ionWorks amplifier from Molecular Devices has noise levels of 10 pA of rms current at 10 kHz bandwidth.

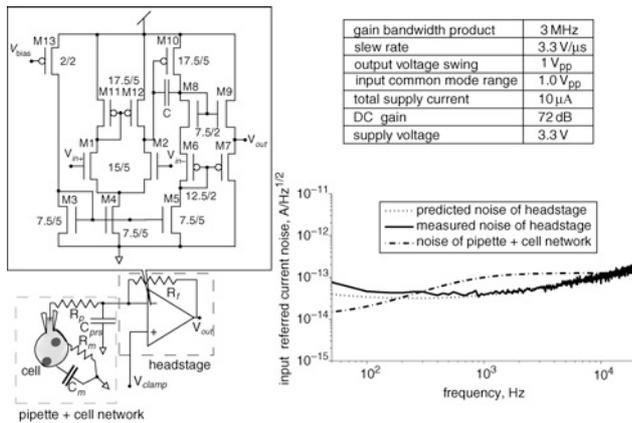


Fig. 4 Operational amplifier characteristics and performance of patch-clamp recording system

Fig. 5 shows recordings made from our patch-clamp system while measuring the ionic conductance of human embryonic kidney (HEK) cells expressing a high density of Slack channels carrying K⁺ current. The left panel shows the time response as control voltage steps (V_{con}) are applied to the cell membrane from -80 to 80 mV in steps of 10 mV. The parasitic compensation was set at 15 pF and the resistive compensation was set at 2 MΩ. The data was sampled at 62.5 kHz and lowpass filtered at 20 kHz. The right panel shows membrane current plotted against control voltage to obtain the cell conductance. The cell conductance was measured as $1/(15 \text{ M}\Omega) = 0.066 \mu\text{S}$. This data exemplifies a typical protocol used in a drug-screening experiment.

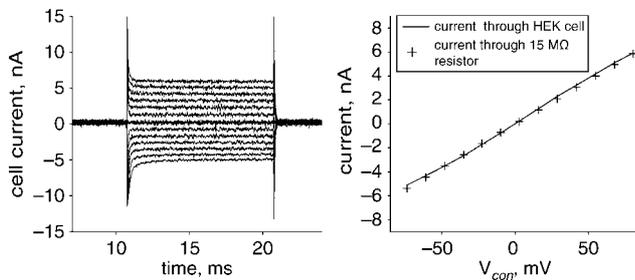


Fig. 5 Whole-cell measurements taken on human HEK cells expressing high density of Slack channels carrying K⁺ current

Conclusion: Implemented in 0.5 μm silicon-on-sapphire technology, the fabricated patch-clamp system occupies 1150 by 700 μm of area and consumes about 3.3 mW of power. The system can record cell membrane currents up to ±20 nA, with an rms noise of 5 pA at 10 kHz bandwidth. The system can compensate for the capacitance and resistance of the pipette electrode, up to 20 pF and 4 MΩ, respectively. Key benefits include the ability to provide accurate low-noise amplification with electrode compensation comparable to bench-top commercial patch-clamp amplifiers.

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