Digital isolation amplifier in silicon-on-sapphire CMOS

E. Culurciello, P.O. Pouliquen and A.G. Andreou

The design and fabrication results of a monolithic four-channel digital isolation amplifier in a 0.5 μm silicon-on-sapphire technology is reported. The isolation device is manufactured in a single die, taking advantage of the isolation properties of the sapphire substrate. The individual isolation channels can operate in excess of 40 Mbit/s using digital phase-shift-keying modulation. Modulation of the input signal is used to increase immunity to errors at low input data rates. The device can tolerate ground bounces of 1 V/μs and isolate more than 800 V.

Introduction: Digital isolation amplifiers are used to communicate an input digital signal from one region to an output digital signal in a second region electrically isolated from the first. An isolation device is conventionally an assembly of two separate circuits packaged together, as in the case of optocouplers [1], capacitive coupling [2, 3], and magnetic coupling using pulse transformers [4]. The isolation of communication pins and output terminals is desirable in environments where ground loops are present, or where it is not possible to ensure a common ground reference between output and input nodes. Typical applications are in harsh industrial environments, military and space applications, high reliability systems, biomedical instrumentation and transportation.

In a conventional bulk process, the isolation of two separate circuits on the same die cannot be obtained because of the presence of a common galvanic substrate. The cost of the isolator is increased owing to the expenses incurred in packaging two dies with the desired isolation properties. In addition, the power consumption is higher owing to the parasitics of multi-chip modules. Multi-chip module isolators use a variety of modulation techniques: FM modulation [5], AM modulation [6], baseband (unmodulated) differential [7, 8].

In this Letter, by taking advantage of the isolation properties of the silicon-on-sapphire (SOS) substrate, we present a monolithic isolator (Fig. 1), that innovates in two ways: (i) it employs a digital phase-shift-keying modulation of the input signals and (ii) it reduces the silicon area and the number of coupling capacitors per channel of our previous implementation. The device uses $N+1$ coupling capacitors for N channels, in contrast to the $2N$ capacitors used in differential implementations [8].

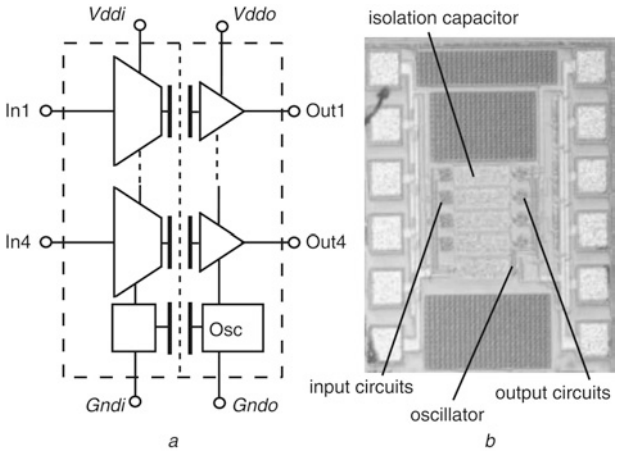

Fig. 1 *System architecture of four-channel digital isolation amplifier and micrograph of fabricated device*

a System architecture
b Micrograph

System description: Fig. 2 is a detailed schematic of one of the four isolation channels named *isoCap3sc*. The specification for each channel required a data rate of 40 Mbit/s, military range temperatures, and input signal rise/fall time between 10 and 1.5 ns. The required isolation was at least 100 V in continuous mode. The device is designed to withstand ground bouncing of more than 1 V/μs using a circuit topology able to reject spurious transitions. This feature is obtained by using digital modulation of the input signal before transmission to the receiver through the capacitive isolation interface of Fig. 2. The use of modulation increases the switching frequency across the coupling capacitor. Spurious transitions are eliminated if the switching frequency is higher than the maximum allowed ground bouncing. The input signal is buffered and modulated at the transmitter (input) side and communicated to the receiver (output) circuit using capacitive coupling. Each stage's coupling capacitor C_f has a capacitance of 150 fF and has been designed using metal-1 and metal-3 plates. The silicon area used by the capacitor is 175×60 μm^2.

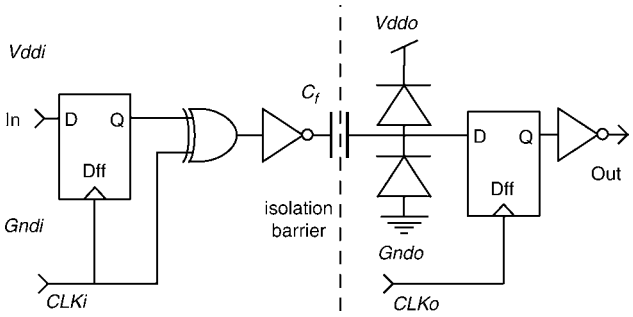

Fig. 2 *isoCap3sc isolation channel*

Our first isolation device [8] used two capacitors per channel, while *isoCap3sc* only uses one capacitor, thus saving silicon area. In addition the previous device provided nonzero bit error rates (BER) at low input rates (6×10^{-7} for a 10 kHz input). Because of the digital modulation, the device here reported did not suffer from bit errors at low frequencies. A 180° phase-shift-keying modulation is performed by XOR-ing the input signal with the transmitter clock *CLKi*. The transmitter clock is obtained through capacitive coupling from the receiver side, where the global clock is generated. We use a 13-stage ring oscillator at the output side to produce an approximately 200 MHz digital clock signal that modulates the input signal. A D-type flip-flop synchronises the modulation and demodulation to avoid spurious transitions of the output due to transmission delay. The input flip-flop operates on the rising clock edge. The demodulator is a flip-flop synchronised to the falling edge of the clock *CLKo*. The output of the *isoCap3sc* isolation channel is the terminal Out in Fig. 2.

To prevent damage due to ground bounces, protection diodes clamp the receiver input node to one of the supplies. The protection diodes are W/L = 5/0.5 μm PL and NL type transistors. The final prototype of the capacitive isolation buffer in Fig. 1*a* (named *isoCap3*) is organised as an array of four independent isolation channels *isoCap3sc* in one single chip. All channels share the same input and output power supplies. Output pads are buffered with digital inverters to be able to drive a 25 pF capacitive load. Other than the protection diodes, all other transistors in the design are of the regular threshold type.

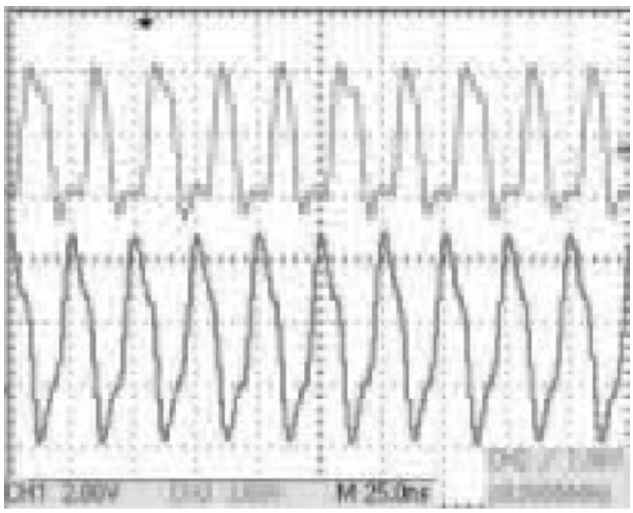

Fig. 3 *Isolation channel input (top trace) and output (bottom trace) operating at 40 MHz*

Results and measurements: We simulated and verified operation (25 Mbit/s) of the isolation buffer, the design corners for temperature

(−55°C, +125°C), and transistor characteristics (typical, fast and slow). We also verified functionality with a power supply of 3.3 V ± 10% of the nominal value at 40 Mbit/s. The measured supply current of four channels in parallel was 1.5 mA at low data rates and 3.3 V power supply. This consumption is attributed to the ring oscillator operating at the receiver's side and generating the global modulation clock. The consumption rose to 4 mA with a 10 MHz input and 16 mA with a 40 MHz input. The majority of the power consumption was due to the output drivers, designed to drive capacitances of up to 25 pF. Fig. 3 shows the output of one isolation channel (bottom trace) when driven with a 40 MHz input (top trace). Operation while providing isolation was verified experimentally, with the circuit operating with an input square wave of 30 MHz, $Vddo =$ 3.3 V and $V_{Gndo-Gndi} = 25$ V.

The measured isolation breakdown of the device occurred in the proximity of 820 V between the grounds of input and output circuits. This isolation is guaranteed by the 3.6 μm of separation from the metal-1 and metal-3 capacitance plates. The breakdown measurements were conducted using an electrophoresis equipment FisherBiotech FB400.

A picture of the fabricated SOS isolator amplifier is given in Fig. 1*b*. The die has 12 bonding pads: the left six are (top to bottom) the input supply, four data inputs and the transmitter's ground; the right six are the output supply, four data outputs and the receiver's ground. Each channel *isoCap3sc* uses $230 \times 6\ \mu m^2$ of silicon area, as opposed to the $230 \times 140\ \mu m^2$ used in our first implementation [8]. Taking into account that one channel *isoCap3sc* is used to transmit the global clock from receiver to transmitter, the four-channel device presented in this Letter uses approximately half of the silicon area of our previous devices.

Acknowledgments: Fabrication was provided by MOSIS. This project was supported by grants NSF-ECS-0225489 and NSF-ECS-GOALI-0010026, also by a NASA Mars Advanced Technology Development grant 1243213.

19 February 2007
Electronics Letters online no: 20070509
doi: 10.1049/el:20070509

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