

Ultra-low Current Measurements with Silicon-on-sapphire Integrator Circuits

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Abstract— This paper reports the results on measurements and modeling of the ultra-low current measurement capability of a silicon-on-sapphire current integrator circuit. We have tested the lowest possible current measurable with the device and the noise performance with pico-ampere input currents. The device is capable of resolving sub-pico-ampere currents with an rms noise of 350fA in a 110Hz bandwidth. The device is also capable of digitally measuring currents up to 100 μ A by employing a pulse-based A/D converters.

I. INTRODUCTION

Integrated current measurement systems are becoming an extremely important integrated circuit component to interface and study physical phenomena at the sub-micro-scale and also for biological research and instrumentation. When venturing in the scale of nano and sub-micron devices and materials, the technological progress is strictly related to the availability and sensitivity of the instrumentation used to characterize the performance of the fabricated structures [1], [2], [3], [4].

In this paper we present an integrating current measurement system for ultra-low-currents. The prototype was fabricated on a 0.5 μ m silicon-on-sapphire (SOS) process. The device employs an integrating headstage with a pulse frequency-modulated digital output. This device was designed as an integrated patch-clamp current amplifier capable of recording from pico- to tens of micro-amperes of current. The high-dynamic range of seven decades and the pico-ampere sensitivity of the instrument was targeted to whole-cell patch-clamp biosensor recordings. We report on the characterization of the ultra-low current sensitivity and noise performance of the fabricated device.

II. CIRCUITS AND SYSTEM OVERVIEW

We have designed the current measuring system based on asynchronous sigma-delta analog-to-digital converters [3]. The sensor is based on a pulsed-output current integrator circuit with reset frequency proportional to the input current [5], [6]. This architecture permits high oversampling ratios at the bandwidths of interest. A block diagram of our current-measuring system is shown in Figure 1.

The input current is integrated over a capacitor until the integrator output reaches either of the compare voltages V_{comp+} or V_{comp-} . At the end of integration, the change in the comparator's state generates a pulse with frequency f_{pulse} . The digital components of the system comprise a

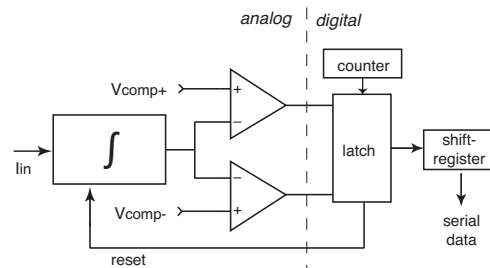


Fig. 1. Integrating current measurement amplifier overview. The analog portion of the circuit integrates the input current up to a positive or negative threshold V_{comp+} and V_{comp-} . After integration, a digital pulse latches a 16-bit counter to produce a digital output.

16-bit counter, latch and shift-register. The counter is free-running, and its value is latched when a pulse from the analog circuitry is detected. This value is then transferred to the shift-registers, and serially communicated to a computer-based data-acquisition system. The time between two integration pulses can be measured accurately with an external clock running at 100MHz. The difference between two latched values thus yields the integrator's reset frequency. This frequency can be used along with the system transfer function in equation 1 to calculate the input current. I_{in} is the input current, C_f the integration capacitance used in the integrator, and ΔV is the voltage swing of the integrator (the difference of V_{comp} and the integrator reset voltage V_{ref}) [3].

$$I_{in} = C_f \Delta V f_{pulse} \quad (1)$$

The single-stage switched-capacitor headstage with single-handed input was used in place of a conventional operational amplifier to reduce the noise reflecting on the headstage input capacitance [3]. If an operational amplifier is used in the design, the input flicker noise level requires the input transistor to be large. This, in turn, forms a large input capacitance where other noise sources would reflect and reduce the overall performance of the amplifier [7].

A schematic of the headstage integrator is shown in Figure 2. The integrator uses a 600fF feedback capacitor C_f to sense the input current [3]. The integrator is initially reset to a reference voltage V_{ref} , chosen to be approximately at the middle of the integration voltage swing. Using a 3.3V supply, V_{ref} is set to 2V, to maximize the integration range. Since the

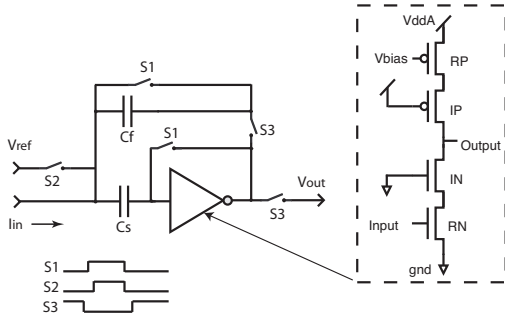


Fig. 2. The silicon-on-sapphire current integrator circuit. During the reset phase, switches S1 and S2 are closed. During the integration phase, switch S3 is closed (in the figure, a high value means closed switch). The gain stage is a cascoded inverter amplifier, and is portrayed in the insert.

system uses correlated double sampling (CDS), two samples are taken for each measurement. The first sample is taken during the reset phase of the system, when V_{ref} is connected to the input of the amplifier and switches S1 and S2 are closed. This voltage is stored on capacitor C_s of 1pF, together with any correlated input noise. The input and output of the inverter are shorted, forcing both nodes to the inverter's logic threshold and highest gain. The second sample is collected during the operating phase of the circuit (switch S3 is closed), when the device is integrating the input current. Since the voltage noise is stored on C_s , the current seen by the integrator is the difference between the samples. Time-correlated noise such as flicker noise is thus partially subtracted from the integration voltage. The integrator's three-phase reset is designed to minimize the charge injection due to simultaneous switching (see Figure 2 for switching sequence). We used compensated switches with dummy half-size transistors. The gain stage is a cascoded inverter amplifier that uses intrinsic transistors (zero-threshold transistor available in the SOS technology) for all the current sources, and to eliminate the need of biases in the cascode. The amplifier input transistor is of the RN kind to allow for modulation of the device current during testing. The amplifier transistors' length and width was $2\mu\text{m}$.

III. MEASUREMENTS AND MODELS

In order to test the device with pico-ampere input currents, we used a very large resistance ($1\text{G}\Omega$ and $10\text{G}\Omega$) to convert a large (volt-level) input voltage into a very low current. The external resistors were soldered to the device input pin, which is set at the V_{ref} voltage by the circuit (see Figure 2). The device was placed in an aluminum box with BNC connectors for external instruments. V_{ref} was set to 2V and the input voltage was varied from 3V to 1V to provide a $\pm 1\text{nA}$ input current swing. This technique is common practice when measuring ultra-low currents.

We used an Opal Kelly XEM3001 FPGA board to collect the digital pulsed data from the current integrator, and we implemented a graphic user interface to display and save the data. The current integrator settings used in the experiment are: $V_{bias} = 1.876\text{V}$, $V_{ref} = 2\text{V}$, $V_{minus} = 1.5\text{V}$, $V_{plus} =$

2.5V . All testing were conducted with $C_f = 600\text{fF}$, and the FPGA timing clock running at 0.2 MHz (at least 200 times the maximum integrator bandwidth).

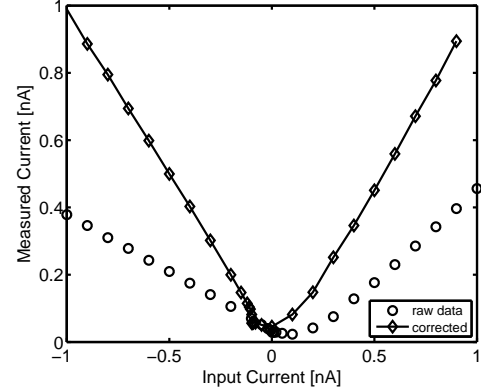


Fig. 3. Transfer function of the current measurement system with an input current of $\pm 1\text{nA}$. The raw data can be compensated for offsets and gain mismatch to report the corrected transfer function (solid line). The input current was injected using a $1\text{G}\Omega$ resistor. The measured current is an absolute value, as the device also provides a digital sign bit.

Figure 3 shows the transfer function of the current measurement system with an input current of $\pm 1\text{nA}$. Each point in the transfer function has been measured 100 times. Reported in Figure 3 is the mean value. This data was collected using a $1\text{G}\Omega$ input resistance. For ease of view, the absolute value of the currents is given in Figure 3, as the device also provides a digital current sign bit. In order to compensate for the device imprecise components, in particular the integration capacitance C_f , we have corrected the transfer function curve to show the linearity of the device. The raw data collected from the device shows an offset of 0.1nA towards positive currents. This offset translates into a 0.1V offset on the comparators threshold voltage. This offset is expected, as the comparators we have used were not designed for low offset voltage. In addition, there is a gain mismatch between the theoretical values (equation 1) and the final results. The positive current raw data was 0.51 times smaller than the measured value, and the negative 0.35 times. This gain mismatch is due to a size discrepancy in the integration capacitance C_f . We have compensated the offset and gain errors, and the resulting transfer function is the 'corrected' data-set in Figure 3.

Figure 4 reports the measured total rms noise from the device. The noise is measured by computing the standard deviation of the 100 samples collected for Figure 3. We have computed a mathematical model of the rms noise of the current integrator. The RMS current noise value $I_{n,RMS}$ can be computed with equation 2.

$$I_{n,RMS} = C_f \Delta V \frac{f_{pulse}^2}{f_{clk}} + \sqrt{kTC_f} f_{pulse} \quad (2)$$

The parameters of equation 2 are: $\Delta V = \|V_{ref} - V_{minus}\| = 0.5\text{V}$, $C_f = 600\text{fF}$ is the integration capacitance, f_{clk} is the counter clock used to measure the pulse frequency, k

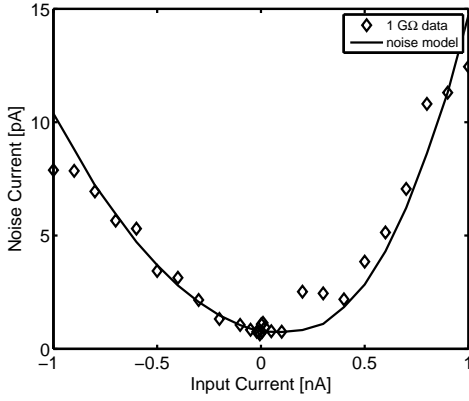


Fig. 4. Measured rms noise of the integrator circuit. The input current was injected using a 1 G Ω resistor. The measured current is an absolute value, as the device also provides a digital sign bit.

is the Boltzmann constant and T is the circuit temperature (room temperature of 25 C). See Figure 2 for details on these components and parameters. Quantization from the counter clock (f_{clk}) is the major source of noise for large currents (>100 pA), together with the kT/C_f component. Low currents (<100 pA) noise is dominated by the integrator thermal noise: $I_{n,thermal}^2 = e_{n,OA}^2(2\pi f_{OA})^2(C_f + C_{in})^2$. $e_{n,OA}$ is the integrator thermal noise, $f_{OA} = 10$ KHz is the integrator bandwidth, $C_{in} = 50$ pF is the input capacitance. The flicker component is reduced by the correlated-double sampling process.

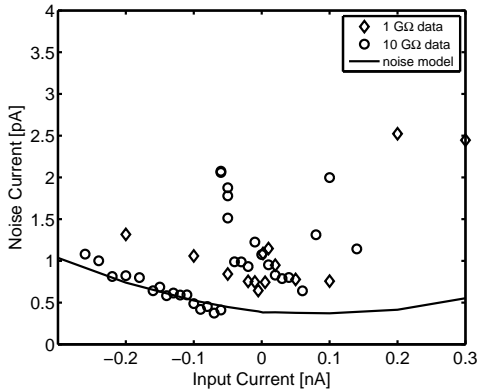


Fig. 5. Measured rms noise of the integrator circuit. Current were injected with a 1 G Ω resistor (diamond) and a 10 G Ω resistor (circles). The measured current is an absolute value, as the device also provides a digital sign bit.

Figure 5 shows a close-up of the noise data in Figure 4 (diamonds), but also reports the data recorded with a 10G Ω resistor (circles). The noise model does not change when a large resistor is used, because the resistor noise is negligible. The model closely matches the data with the larger resistor (see circles on the left side of Figure 5), which helps to reduce external noise and lower the thermal noise component. The matching is very adequate for the negative currents, while the noisier data collected for positive currents does not provide for a good match with the model. This is also visible in the

lower right portion of Figure 4. The model, however, matches the data well in the whole range of Figure 4, confirming its validity. Finally we should note that the results measured in this paper should be compared with the interpretation given in reference [5], which states that the major cause of noise is shot noise from the reference current source. Our system does not use a current source, so it offers even better noise performance. As can be seen in Figure 5, at least for negative currents, the rms noise is less than 350fA with an input current of 50pA and a bandwidth (f_{pulse}) of 110Hz. This is one of the highest sensitivity values obtained with an integrated current integrator circuit, and the first one designed in the silicon-on-sapphire process.

IV. CONCLUSIONS

We have measured and modeled the noise of an asynchronous current integrator fabricated in the silicon-on-sapphire fabrication technology. We show that very good performance of the current measuring device, with an rms noise of less than 350fA with an input current of 50pA and a bandwidth (f_{pulse}) of 110Hz. The current sensitivity by bandwidth product is one of the best to-date obtained with an integrated current integrator. This device can be used for ultra-low current measurement in biological sensor interfaces and nano-scale device sensing.

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