Three-Dimensional Photodetectors in 3-D Silicon-On-Insulator Technology

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***Abstract*—We report on the design and measurement results of three-dimensional (3-D) photodetectors in a 0.18-μm silicon-on-insulator technology. The device measurements reported here show that the photodetectors can be used for the design of high-density imaging arrays in 3-D CMOS fabrication processes. The photodiodes respond to light in the range of 1–200 000 lx with currents of 2 fA to 300 pA and can be arranged in a 3-D stack. The phototransistors respond to light intensities of 5–200 000 lx with currents from 50 fA to 2.3 μA.**

***Index Terms*—Photodetector, photodiode, phototransistor, silicon-on-insulator (SOI), three-dimensional (3-D) integration.**

I. Introduction

THREE-DIMENSIONAL (3-D) integrated-circuit technologies promise to offer integrative advantages in the vertical dimension for stacking both homogenous and heterogeneous layers of conventional CMOS dies [1]–[3].

Recently, heterogeneous imaging sensor arrays have been presented with a million vertical connections between dies [4]. This array was obtained by wafer stacking a 0.35-μm silicon-on-insulator (SOI) CMOS on top of 0.35-μm bulk CMOS for the design of the photosensitive elements. The bottom layer die was thinned to allow backlight illumination to reach the detectors, and mounted on a glass substrate for mechanical stabilization. The main reason for the use of a combination of bulk CMOS and SOI CMOS, was the unavailability of photodetectors in SOI CMOS.

The purpose of this letter is to present design and measurements obtained from native SOI photodetectors fabricated in the first available 3-D multiproject run offered by Massachusetts Institute of Technology (MIT) Lincoln Laboratories. A cross section of the Lincoln Labs 3-D die stack is given in Fig. 1. Two thinned SOI dies (tiers 2 and 3) are stacked upside down on top of another die (tier-1). Vertical interconnects are obtained by means of a low-temperature metallization process. The contribution of this letter is to: 1) present photodetectors obtained with native rules on the 3-D SOI process and 2) show a stack of photosensitive SOI devices capable of imaging light in the vertical dimension and in multiple silicon active layers.

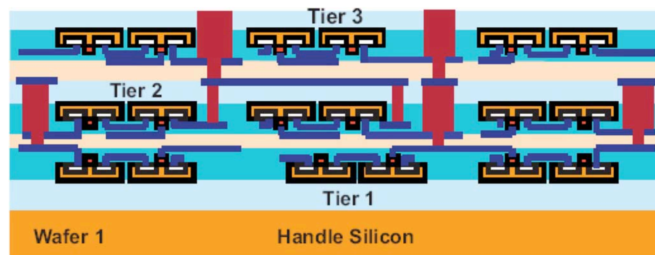

Fig. 1. Cross-section of the MIT Lincoln Laboratories 3-D integration of three SOI dies.

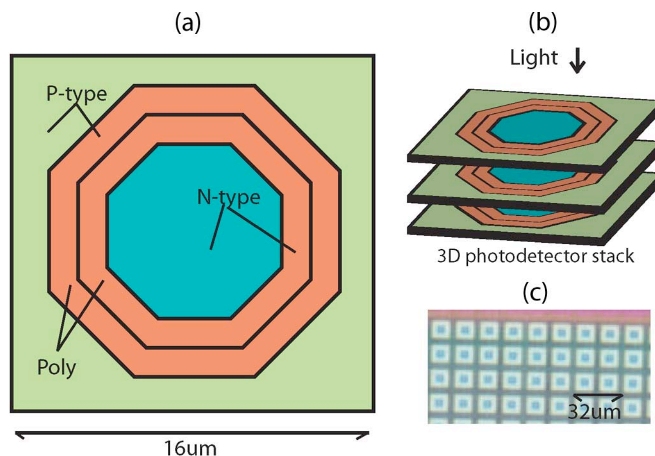

Fig. 2. (a) Layout of the fabricated photodiode and phototransistor. (b) 3-D arrangement of the detectors. (c) Closeup micrograph of the fabricated array of photodiodes.

Our devices allow to use the standard SOI layer as photodetector layer for the design of vertically integrated image sensor arrays. These devices also eliminates the need of heterogeneous integration of bulk CMOS dies and the need of die-thinning techniques to image light. The photodiode is also the first SOI photosensitive device to have been integrated in a large 3-D image sensor array.

II. Photosensitive Devices

The SOI photodetectors presented in this letter are presented in Fig. 2(b). They are implemented as a stack of three thin-film SOI silicon layer (50 nm). These three active layers are separated by field oxide of 7.5 μm between top and middle, and 12 μm between middle and lower. The detectors have been fabricated by MIT Lincoln Laboratories, therefore process parameters as layers thickness and organization cannot be

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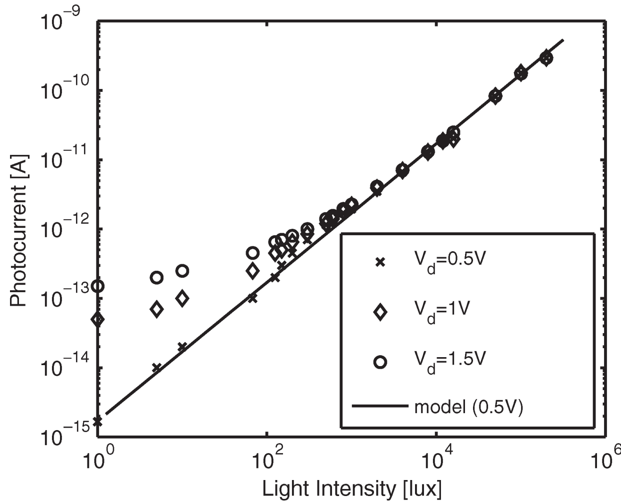

Fig. 3. Responsivity of the top-layer 3-D SOI photodiode. The photodiode area is 16×16 μm^2. The QE for the photodiode is 0.0037 at a 0.5-V bias. The dynamic range of this detector is more than five orders of magnitude of light intensity.

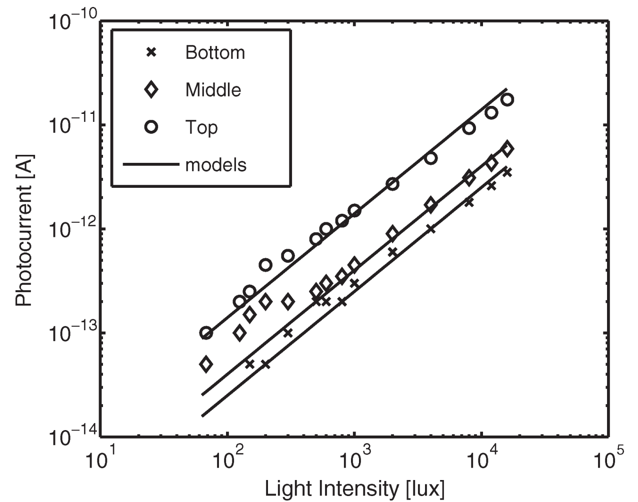

Fig. 4. Responsivity of a 3-D stack of SOI photodiodes. The three active layers are separated by 7.5 μm between top and middle, and 12 μm between middle and lower.

modified. We verified operation of three photodetectors in the 3-D process: a top-layer photodiode, a 3-D photodiode stack, and a phototransistor.

The photodiodes are obtained abiding N- and P-type silicon regions and feature a vertical junction. In order to optimize the detectors for maximum dynamic-range, we took particular care in the layout to avoid possible causes of leakage currents at the diode junction. The layout of the detector is circular, to avoid interfaces between the N- and P-type and the deposited local oxidation of silicon. For the same reason, the photodiode has been gated with a polycrystalline silicon layer to avoid having deposited silicon oxide above the diode. The polylayer insures a low-leakage thermally grown oxide layer and thus prevents the interface currents that plagued previous SOI photodetectors [5], [6]. Fig. 2(a)—left shows a layout of the 3-D photodiode, with an area of 16×16 μm^2. Fig. 2(c) is a micrograph closeup of a 9×4 array of such photodiodes. These detectors have been used to design and fabricate a 97×97 pixels 3-D image sensor (details in a forthcoming publication).

We also designed a vertical stack of photodetectors in the 3-D process. This device has been obtained by overlapping three photodiodes obtained in each of the available active silicon layers of the 3-D fabrication process [Fig. 2(b)].

Finally, we have also designed and measured an N-type phototransistor in the 3-D process. The phototransistor has the same circular layout and dimensions of the photodiode in Fig. 2(a). The phototransistor gate (polysilicon layer) was left floating. P-type phototransistors and all other photodetectors without the CBN/CBP process layers did not provide any photosensitivity. The CBN/CBP layers are the transistor channel implants in the 3-D process. The CBN/CBP channel doping is of $5 \cdot 10^{17}$. This layer was not used in the layout of the photodiodes to maximize the depletion region and thus the photon collection efficiency.

III. Results and Measurements

Photocurrent data was collected with a picoammeter unit. We used a conventional halogen broad-spectrum (white) light as a source, since the final application is the use of this sensor for indoor lighting. The light meter was a commercial photographic unit with a range of 1–20 000 lx. We used neutral density filters to measure high light intensities. Also, 1.5 V is the nominal supply voltage rating of the 3-D process.

Fig. 3 shows the data collected from the phototransistor placed in the topmost layer of the 3-D process. We have biased the phototransistor at 0.5, 1, and 1.5 V. There is no significant difference between the bias voltages of the photodiode and its influence on the photosensitivity at light intensities higher than 200 lx. The different biasing conditions manifest themselves on the photodiode responsivity in the form of an higher dark current (and deviation from the linear model). At higher bias voltages, the electric field in the depletion region of the diode is sweeping a larger number of thermally generated carriers to the diode terminals [7]. We computed a model of the diode photocurrent as: $I_{\mathrm{ph}} = I_{\mathrm{in}} \cdot 1.7 \cdot 10^{-15}$, where I_{in} is the incident illumination power in lux. The model corresponds to a Responsivity of 0.0016 at 535 nm.

We also measured the external quantum efficiency (QE) for the photodiode of 0.0037 at a 0.5-V bias. We calculated the QE as the ratio between the photodiode current and the incident optical power at the detector (in watts) at 535 nm. The low QE is due to the shallow thickness of the SOI silicon layer (50 nm) and the vertical junction, both contributing to a small active photosensitive region.

Fig. 4 reports the data collected from the stacked 3-D photodiode device. Since light is traveling in the vertical dimension through the three-layer stack (top, middle and bottom), the responsivity of the lower layers is reduced. The photocurrent models are, respectively: $I_{\mathrm{top}} = I_{\mathrm{in}} \cdot 1.4 \cdot 10^{-15}$, $I_{\mathrm{mid}} = I_{\mathrm{in}} \cdot 0.4 \cdot 10^{-15}$, and $I_{\mathrm{bottom}} = I_{\mathrm{in}} \cdot 0.25 \cdot 10^{-15}$. The data in Fig. 4 has been obtained with a bias voltage of 0.5 V. Notice that most of light is lost to the top layer, where the highest energy is absorbed. The inefficiency of the 50-nm silicon layer in transducing low-energy intensities makes the lower two layers have similar responsivities.

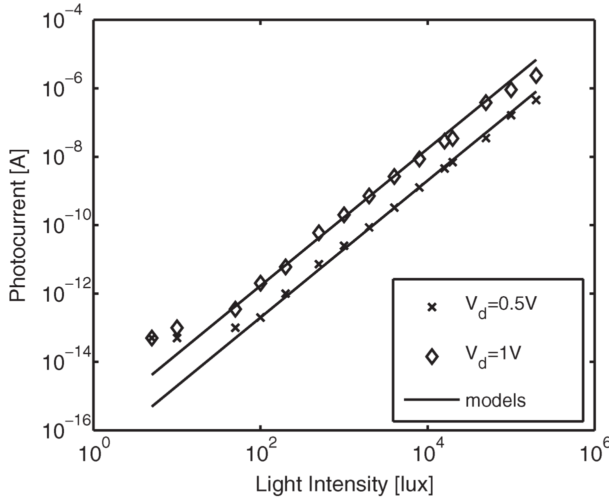

Fig. 5. Responsivity of the MOS top-layer phototransistor. The MOS photocurrent is proportional to the square of the incident light power. The dynamic range of this detector is more than four orders of magnitude of light intensity.

Finally, in Fig. 5, we report on the responsivity of the 3-D phototransistor of the topmost layer. Notice that the photocurrent almost reaches the saturation current for this device (2.36 μA) at 200 000 lx with 1-V bias. We computed a photocurrent model as: $I_{0.5V} = I_{\text{in}}^2 \cdot 1.7 \cdot 10^{-16}$ and $I_{1V} = I_{\text{in}}^2 \cdot 2 \cdot 10^{-17}$. In this MOS structure, the photocurrent is proportional to the square of the incident light power. This power law is due to two combined effect: 1) the light-induced generation of carriers in the device body and 2) the resilience of majority carriers in the device body [8, p. 78]. Equation (1) shows the dependance of the body voltage on the incident illumination ($V_{\text{bs}} = V_{\text{th}} \log(I_{\text{in}}/I_{\text{in0}})$) [8, p. 80], with I_{in0} being the dark-generated photocurrent. I_s, k_1, k_2, k_3 are bias and process merged constants, V_{th} is the thermal voltage

$$I_{\text{ph}} = I_s e^{\frac{V_{\text{bs}}}{V_{\text{th}}}} = k_1 I_{\text{in}} e^{V_{\text{th}} \log\left(\frac{I_{\text{in}}}{I_{\text{in0}}}\right)} = k_3 I_{\text{in}}^2. \qquad (1)$$

IV. Conclusion

We have designed and measured photodetector devices in a 3-D SOI process. The photodiodes respond to light in the range of 1–200 000 lx with currents of 2 fA–300 pA and can be arranged in a 3-D stack. The phototransistors respond to light intensities of 5–200 000 lx with currents from 50 fA to 2.3 μA. The photodetectors presented in this letter provided a large dynamic-range in light intensities and can be used for the design of imaging arrays in 3-D SOI processes.

Acknowledgment

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