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A monolithic isolation amplifier in silicon-on-insulator CMOS: Testing and applications

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Abstract In this paper, the design and test results of a 4-channel digital isolation amplifier are presented, along with results of a prototype power converter circuit using the amplifier for voltage feedback regulation. The amplifier uses a capacitive coupling technique to transfer digital signals from input to output while preserving galvanic isolation between the two. The isolation amplifier was fabricated in a 0.5 μm Silicon-on-Sapphire (SOS) technology and uses the isolation properties of the SOS substrate to achieve more than 800 V isolation between input and output grounds. Each of the four channels can operate in excess of 100 Mbps using a differential transmission scheme to reject ground bounce transients up to 1 V/μs. The input circuit can be powered from an on-chip charge-pump to permit single supply operation. The device can be used in a wide variety of applications that require passing signals across an isolation barrier: power supplies, remote sensing, and medical and industrial applications.

Keywords Isolation · Isolator · Capacitive coupling · SOI · SOS · Non-galvanic

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1. Introduction

Galvanic isolation between circuits is often required to protect circuits from high-voltages and to prevent noise spikes from coupling onto sensitive analog and digital circuits. In applications where a common ground cannot be guaranteed, it can prevent ground loops from causing circuit damage and offset errors at sensitive nodes. When signals must be transmitted across an isolation barrier (e.g. power supply feedback signals, command and control signals, etc.) two principal methods are used: optocouplers and magnetic coupling using pulse transformers [1–3]. Both of these options, however, have important drawbacks that limit their effectiveness in certain applications. Optocouplers have demonstrated strong susceptibility to noise injection, low bandwidth, and high static power consumption [4]. In addition, their current transfer ratio (CTR) varies significantly from part to part and with respect to time, temperature, operating current and radiation exposure [5, 6]. Magnetic coupling offers greater stability and wider bandwidths than optocouplers but at the cost of additional modulation/demodulation circuitry needed to pass DC signals across the isolation barrier. Unfortunately, the size of transformers and the complexity of the modulation circuitry are limiting factors in many applications.

Capacitive coupling schemes offer a third alternative for communicating across an isolation barrier. Unlike optocouplers, capacitive coupling does not degrade with respect to temperature or radiation exposure. Power consumption is dependent on the size of the coupling capacitor and the frequency of signals to be transmitted and is typically much smaller than that of optocouplers. In addition, unlike magnetically coupled schemes, the entire capacitively coupled circuit can be fabricated on a single integrated circuit to significantly reduce board space requirements. Capacitive

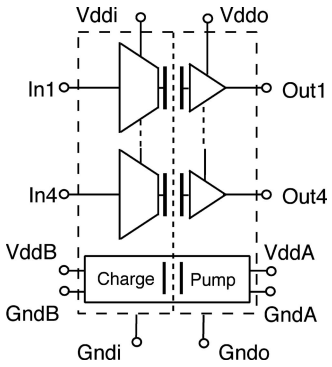

Fig. 1 System architecture: 4-channel isolation buffer. *(2 channels not shown)*

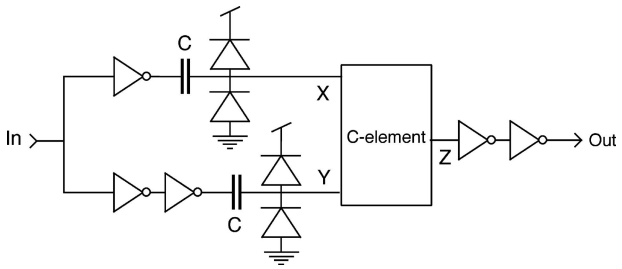

Fig. 2 One of four identical capacitive isolation circuits used in the device: the isolation cell *isoCap2sc*. Using a differential transmission scheme, the signal and its complement are capacitively conveyed across an isolation barrier given by capacitor C. A c-element circuit recombines the differential signals into the output

coupling has been employed in bulk CMOS multi-chip modules to transfer data signals between multiple dies [7–9]. Capacitive coupling has also been used to pass data between isolated sections of a single die using a Silicon-on-Insulator (SOI) substrate [10]. In addition, the authors recently reported on a Silicon-on-Sapphire (SOS) device that employs the technique to couple signals across an isolation barrier at up to 100 Mbps data rates [11, 12]. Capacitive coupling can be also used to transfer data and power in a 3D assembly of two SOS dies with no galvanic connections [13].

In this paper, we expand the discussion of our 4-channel isolation buffer whose architecture is shown in Fig. 1. We discuss theory of operation, provide measured results on the fabricated device, and report on a unique power supply application of the isolator. The paper is organized as follows: Section 2 discusses the general architecture and operation of the device while Section 3 provides a more detailed analysis of the capacitive coupling model. Section 4 gives some important results of tests applied to the device including results over the full temperature range (-55°C to $+125^{\circ}$C). Finally, Section 5 describes an application of the isolation amplifier for implementing closed loop control in isolated power converter applications. Measurements of line and load regulation for the prototype converter and improvements over other topologies are discussed.

2. System overview

The monolithic isolation amplifier is a four channel device fabricated on a Silicon-on-Sapphire (SOS) substrate. The device was designed to operate at data rates of up to 100 Mbps on all four channels with at least 100 V continuous isolation between input and output grounds. The device is designed to withstand ground bounce transients of more than 1 V/μs by using asynchronous circuitry to reject spurious transitions. This property is obtained by employing a differential scheme at the input, before the capacitive isolation interface as shown in Fig. 2. The coupling capacitors C have a capacitance of 150 fF and have been designed using metal-1 and metal-3 plates. The silicon area used by the capacitor is $175 \times 60\ \mu\text{m}^2$. Section 3 provides a detailed rationale for this capacitance selection.

The differential signals are buffered and capacitively coupled across the isolation barrier where they are recombined using the asynchronous c-element cell *celiso* shown in Fig. 3. The C-element circuit is a static logic cell that switches its output only when it detects a valid differential transition. This is defined as a transition where one output has a logic level 1 and the other level 0. If only one of the inputs switches (for example because of a ground bounce or noise spike), the output will not toggle in response. This function can be expressed in Concurrent Hardware Process (CHP) production rules by equation:

$$[\neg X \wedge Y] \rightarrow Z\uparrow, [X \wedge \neg Y] \rightarrow Z\downarrow \tag{1}$$

The unit can be powered from input and output side or, alternatively, from the output side only. In the latter configuration, an isolation charge pump operating off the output power supply provides power to the input differential circuitry [14]. The charge pump, based on the Dickson charge pump [15], is shown in Fig. 3. An isolation charge pump architecture has the same functional blocks as a conventional charge pump but with the power supply rails of the oscillator galvanically isolated from the output supply rails. The charge pump was designed to provide an isolated power supply identical to the input supply to a galvanic isolation buffer. The circuit works by pumping charge along the diode chain as the capacitors are successively charged and discharged during each clock cycle. An eleven stage ring oscillator produces a 350 MHz square-wave clock signal to drive the pump. The output of the oscillator is buffered to drive the pumping capacitances C. Each capacitance has a value of 450 fF and forms an isolation barrier between the two regions of the circuit. These capacitors are designed using a parallel plate configuration of metal-1 and metal-3 (plate separation of 2 μm SiO_2 dielectric) and are comprised of three parallel units

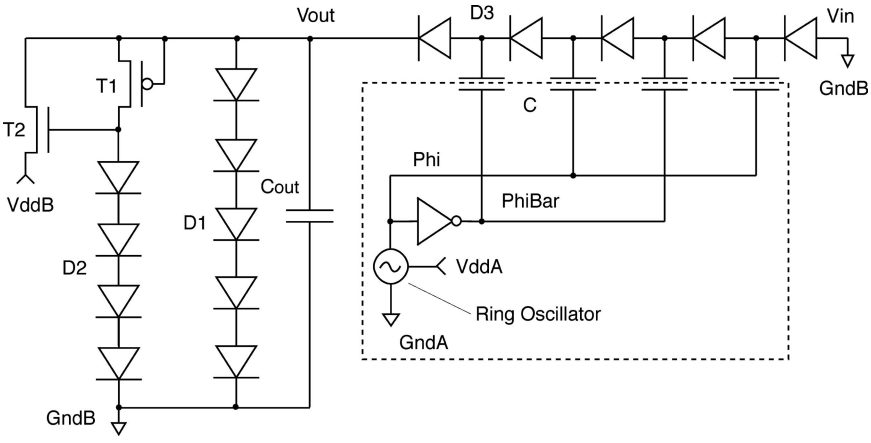

Fig. 3 A four-stage Dickson charge pump is used to power the input side of the isolator from the output side. The device uses an internal digital clock to pump charge across the same isolation capacitors *C* of Fig. 2

of the same isolation capacitors used in the isolation circuit *isoCap2sc*.

To optimize the design of the Dickson charge pump circuit, we employ MOS transistors with different threshold voltages that are available in the Peregrine SOS CMOS process [14, 16]. The following naming convention is employed to identify the device:regular *Rx* threshold ($V_{\mathrm{TH}} \approx 0.7$ V), low *Lx* threshold transistors ($V_{\mathrm{TH}} \approx 0.3$ V, and intrinsic *Ix*, zero threshold transistors ($V_{\mathrm{TH}} \approx 0$ V). The type of transistor is denoted by substituting *x* for either N or P. Diodes D1 are diode connected regular threshold transistors that are employed by the technology vendor as ESD protection diodes.

Diode connected NL MOS transistors are used as the rectifiers (D3) in each pump stage. The use of a low threshold MOS transistor in this part of the circuit minimizes the forward bias diode drop V_D to 0.3 V, and reduces the undesirable voltage drops on the rectifiers. A 9 pF capacitor at the output (C_{out}) together with a series of 5 diodes (D1) are used as the charge pump filter and constrain the maximum voltage within the maximum supply range of the process (3.3 V). Transistors T1, T2 and a diode chain of four diodes D2 form an active voltage regulator at the output of the charge pump to produce the regulated voltage *VddB* (Fig. 3). The series regulator transistor T2 is a zero threshold IN device biased by a string of four regular threshold (RN) diode connected MOS transistors (D2) and a current source. Transistor T1 is a self-biased current source implemented using an IP MOS transistor. Transistor T2 acts as an ideal voltage follower without a build-in voltage. The device type and sizes are given in Table 1.

The pump generates the required 3.3 V input supply in order to drive the inputs at 100 MHz. Protection diodes ensure that an unbounded received voltage does not damage the input circuits. The charge pump has separate external supply connections and can be disabled to save power when the input side is externally powered.

The isolation amplifier's inputs are clamped to the supply rails through protection diodes. Its outputs are buffered with

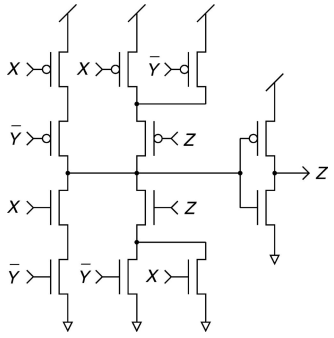

Fig. 4 Asynchronous c-element cell for the capacitive isolator: *celiso*. The output *Z* of this circuit switches only if one of the input *X* or *Y* switches. When both input switch at the same time the output *Z* does not change

digital inverters to drive 50 pF capacitive loads. The final prototype is organized as an array of 4 separate isolation channels (each made up of one *isoCap2sc* cell) and sharing the same input and output power supplies. A micrograph of the final device layout is shown in Fig. 5. The die has 16 bonding pads: the bottom eight are (left to right) two input supplies (supply for the input isolation circuit and output of the charge pump), four data inputs and two grounds (circuit and charge pump output ground), the top eight are (left to right) the two output supplies (output circuit supply and charge pump input supply), four data outputs and two grounds (output circuit ground and charge pump input ground).

Table 1 Device type and size of MOS transistors used in the charge pump design

Device	Type	Size (μm)
D1	RN	27.4/1.6
D2	RN	2/2
D3	NL	15/0.5
T1	IP	10/2
T2	IN	6/4

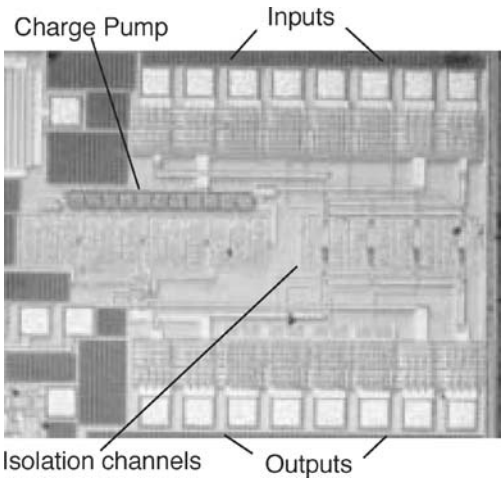

Fig. 5 Micrograph of the fabricated SOS isolation amplifier

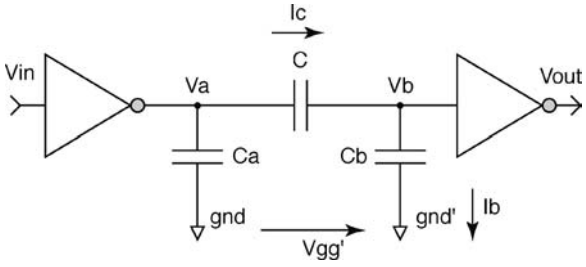

Fig. 6 Model of operation of a capacitively coupled isolation circuit

3. Capacitive coupled isolation circuit model

To ensure proper operation of the capacitive coupled isolation circuit, the isolation capacitance C must be much higher than the receiver input capacitance C_b. This is apparent from an examination of the model shown in Fig. 6, from which we can write an equation for the voltage at node V_b:

$$V_b = V_a \frac{C}{C + C_b} \tag{2}$$

Equation (2) makes it immediately clear that if we wish to avoid attentuation at node V_b and prevent transmission errors, we must first ensure that $C \gg C_b$.

But there is a second important consideration that affects the design of the isolation amplifier, namely that input voltage swings have to be detected while ground bounce swings have to be rejected. In fact only the former is the desired signal, while the latter is a noise signal. Given a fixed parasitic capacitance C_b and the fact that C must be chosen much larger than C_b according to Eq. (2) above, we shall see that an important restriction is placed on input signal slew rate.

We begin by considering the factors that affect the received voltage at node V_b. If we assume that $C \gg C_b$, then the rate of change in voltage V_b is dependent on two quantities: the time derivative of voltage V_a (in turn governed by the input voltage V_{in}) and the time derivative of the ground bounce voltage $V_{gg'}$. This is concisely written as Eq. (3):

$$\frac{dV_b}{dt} = f\left(\frac{dV_{gg'}}{dt}, \frac{dV_a}{dt}\right) \tag{3}$$

We can rewrite Eq. (3) in terms of the current through capacitor C_b:

$$i_b = C_b \frac{dV_a}{dt} - C_b \frac{dV_{gg'}}{dt} \tag{4}$$

Therefore, in order to maintain correct device operation, it is clear that the input slew rate must be much larger than the ground bounce slew rate:

$$\frac{dV_a}{dt} \gg \frac{dV_{gg'}}{dt} \tag{5}$$

If Eq. (5) is satisfied, then the ground bounces can be attenuated using a high-pass filter at the receiving node. The isolation amplifier includes a small leakage path at the receiver node for this purpose. The leaky node dissipates accumulated ground bounce charge without affecting the intended charge deposition due to a valid input transition.

As an example, consider an application where the device operates at a data rate of 10 Mbps from a 3 V power supply with a maximum specified ground bounce of 1 V/μs. The worst case minimum input slew rate $(dV_a/dt)_{\min}$ is then 60 V/μs (corresponding to a triangular input waveform). It is clear that under these conditions, Eq. (5) is well satisfied and reliable device operation is ensured.

4. Results and measurements

We conducted a series of tests to quantify the device performance in a variety of operational configurations and several temperature conditions (-55°C, $+25^\circ$C, and $+125^\circ$C). We began by verifying the isolation property of the device which was specified as a continuous ground-to-ground isolation of at least 100 V. We used a Keithley 236 unit to measure current draw as the potential difference between the two grounds was varied. Figure 7 shows that no significant increase in current was observed up to a 110 V potential difference which verifies the device meets the isolation requirement. The actual *measured* breakdown of the device occurs in the proximity of 820 V between the grounds of input and output circuits. This isolation is guaranteed by the 3.6 μm of separation from the metal-1 and metal-3 capacitor plates. The breakdown measurements were conducted using an electrophoresis equipment FisherBiotech FB400.

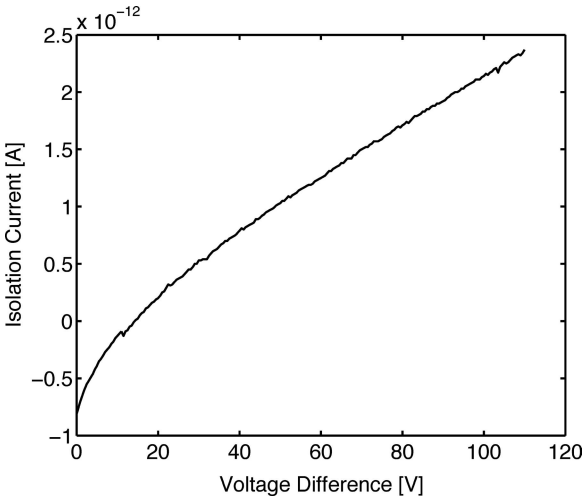

Fig. 7 Isolation performance between metal-1 and metal-3 in the SOS process

We next measured device supply current (with and without the charge pump operating) versus supply voltage versus number and frequency of channels operating. These results are summarized in Table 2.

Next, we determined the minimum permissible input slew rate for error free transmission. We defined this as the lowest slew rate for which the output would still consistently toggle. For fast edges, the capacitor current i_C is much larger than the leakage currents at the leakage node which keeps V_b relatively unattenuated. But as the input edge rate slows, leakage currents become a larger fraction of i_C and V_b begins to become attenuated. At some critical level of input edge rate, the received voltage will be too small to commute the output buffer and a transmission error will occur.

Table 2 Measurements of device current for various power supply and input signal configurations

$V_{DD_{in}}$	$V_{DD_{out}}$	I_{DD}(mA)	Input signal(s) (MHz)
2.5	$V_{DD_{in}}$	0.1055	1 at 1
2.5	$V_{DD_{in}}$	0.2257	4 at 1
2.5	$V_{DD_{in}}$	4.789	1 at 80
2.5	$V_{DD_{in}}$	15.980	4 at 80
3.3	$V_{DD_{in}}$	0.2539	1 at 1
3.3	$V_{DD_{in}}$	0.6684	4 at 1
3.3	$V_{DD_{in}}$	5.956	1 at 80
3.3	$V_{DD_{in}}$	24.94	4 at 80
2.5	CP	1.620	1 at 1
2.5	CP	1.738	4 at 80
2.5	CP	6.302	1 at 1
2.5	CP	17.545	4 at 80
3.3	CP	3.4978	1 at 1
3.3	CP	3.6751	4 at 80
3.3	CP	9.833	1 at 1
3.3	CP	25.280	4 at 80

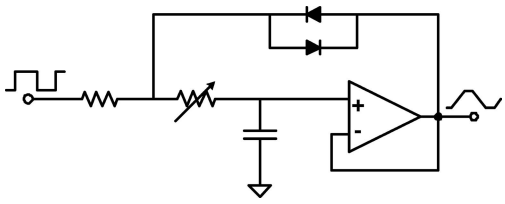

Fig. 8 Adjustable slew-rate limiter circuit used to determine the isolator's minimum acceptable slew rate

To find this critical rate, we used the circuit of Fig. 8 and a 10 Hz 50% duty cycle square wave input to create an adjustable, slew rate limited input for the isolator. We then ramped the slew rate down until we found the minimum rate at which the device would still reliably operate. We found that this rate varied significantly among devices from a minimum of 0.01 V/μs to a maximum of 0.2 V/μs. The average measurement was 0.067 V/μs. These results are in good agreement with specifications of standard logic interfaces. For example, a typical interface device might be the HC14 Schmitt trigger inverter with minimum specified output slew rate of 18 V/μs. This is 90 times faster than the minimum rate recognized by the isolation amplifier and implies good margin in the interface.

We performed an end-to-end system test by calculating bit error rates through the device with operating temperature and ground bounce slew rate as parameters. The isolator was powered from 3.3 V input and output supplies with the charge pump disabled. We used a Fireberd 6000 bit error rate tester (BERT) to inject a pseudo-random data sequence into the device and record errors in the output sequence. The pseudo-random sequence was 2047 bits long and clocked at a frequency of 15 MHz. We connected a variable frequency sawtooth waveform between the isolator's input and output grounds to measure ground bounce rejection. The sawtooth had a 20 V_{pp} amplitude with 50% duty cycle and a variable frequency that we set to give ground bounce slew rates ($dV_{gg\prime}/dt$) from 1 V/μs to 12.5 V/μs. Since the BERT has common input and output ground connections, we used pulse transformers to couple the clock and data signals between the tester and the isolator to avoid shunting the ground bounce signal. Average bit error rates were calculated after 1×10^9 transmitted bits. The complete setup is shown in Fig. 9.

The test was first performed at room temperature and then again at the military temperature extremes (−55°C and +125°C). Figure 10 shows the number of received bit errors as a function of ground bounce slew rate ($dV_{gg\prime}/dt$). It is readily apparent from these results that the device easily meets the 1 V/μs ground bounce rejection requirement over the full military temperature range.

Lastly, we performed a measurement of the loading and supplying performance of the charge-pump circuit. The measured unloaded charge pump voltage output *VddB* was

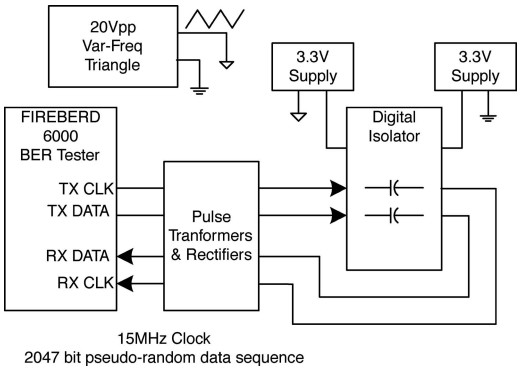

Fig. 9 Test setup for measuring bit error rate vs ground bounce slew rate

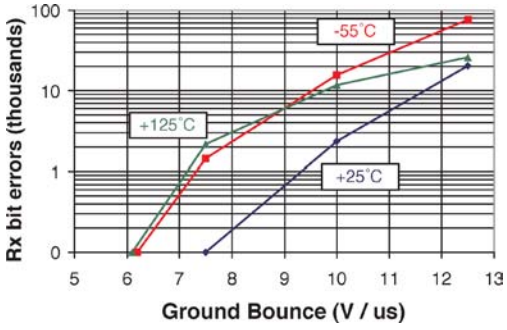

Fig. 10 Number of received bit errors vs. ground bounce slew rate

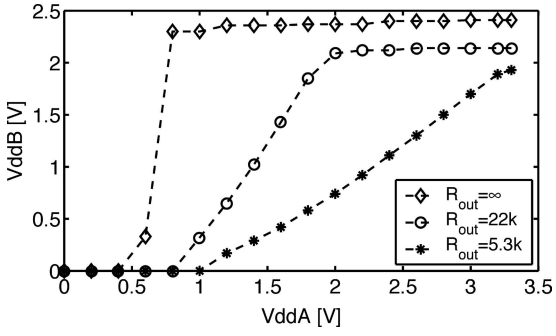

Fig. 11 Received voltage output of the charge pump as a function of the load

2.68 V. The output voltage is limited to this value by the chain of protection diodes D1 in Fig. 3. Figure 11 plots the measured charge pump output voltage (*VddB*) as a function of the input power supply (*VddA*) and the load. The charge pump was tested with three loading conditions: unloaded, loaded with 5 kΩ and with 22 kΩ resistors. Using an input power supply *VddA* of 2 V the charge pump can supply 100 μA at 2 V for a 22 kΩ load or 0.6 V for a 5.3 kΩ load. The output of the charge pump falls rapidly when the current drawn is high or the input voltage is too low to counterbalance the losses in the charge pump diodes. The power consumption of the unloaded charge pump circuit is 2.5 mA at 3.3 V supply. The current consumption is due to the oscillator circuit and the buffers to drive the pumping capacitors.

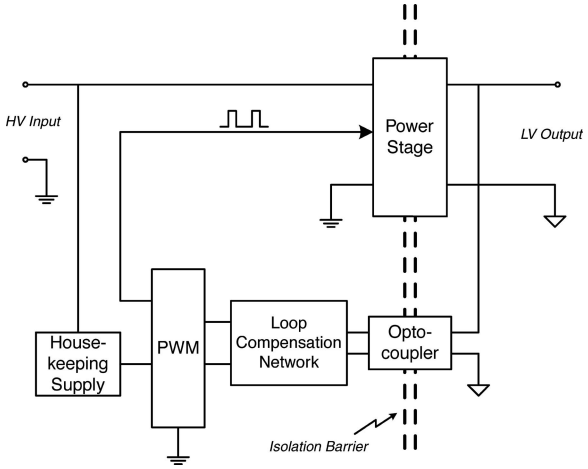

Fig. 12 A typical isolated DC/DC converter architecture. The PWM senses the ground isolated output voltage through an optocoupler and drives the power stage as needed to keep the output voltage constant

5. Application: Isolated power supply feedback

One of the most common applications requiring input/output galvanic isolation is power conversion. AC/DC and DC/DC converters accept a high voltage (HV) bus input and convert it down to one or more low voltage (LV) secondary outputs which are regulated against changes in line voltage and output loads. Although several converter architectures have been proposed, nearly all share a common need to pass control signals across the isolation barrier, either in the form of a DC error signal or an AC drive signal. An example of a *typical* power converter architecture is given in Fig. 12. In this scheme, a pulse width modulator (PWM) controller located on the input side of the isolation barrier closes the loop around a voltage feedback signal derived from the output side. The PWM drives the main switch with a fixed frequency train of variable width pulses which chops the input into a pulse train whose average voltage just equals the desired output voltage. As the output voltage changes as a result of input or load changes, the loop servoes the pulse width to keep the average voltage constant and therefore regulate the output voltage. The traditional choice for feedback across the isolation barrier is optocoupling because of its simple implementation and linear transfer function. However, as noted previously, optocouplers suffer from variations in CTR and low bandwidth which limits the performance of the resulting power converter. To improve performance and reliability, magnetic coupling can be used in place of optocouplers at a penalty of increased parts count and design complexity.

The isolation amplifier provides a third alternative to these coupling schemes, offering simplicity, robustness, and excellent performance. To illustrate how this can be achieved, the traditional architecture of Fig. 12 has been modified as shown in Fig. 13. Here, the PWM is located on the output

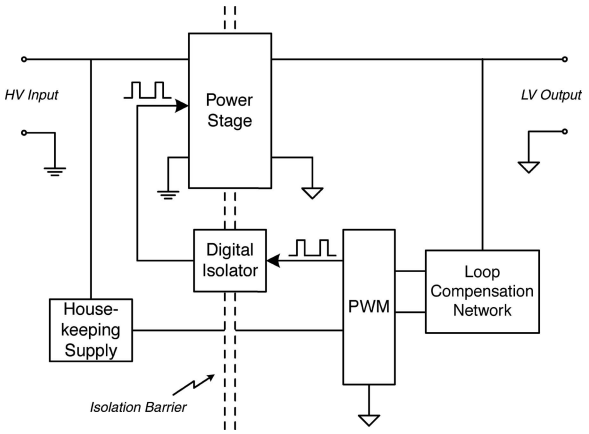

Fig. 13 An alternative to the traditional DC/DC converter architecture. Here, the PWM is located on the output side of the isolation barrier for improved output voltage regulation. The isolation amplifier couples the PWM's output pulses back to the input side to drive the main power stage

side where it directly senses the output voltage and compares to a reference to generate a pulse width modulated drive signal. The isolation amplifier then transmits this signal back to the input side where it drives the main switch (through a high power driver circuit), coupling energy through the main transformer to the output load(s). This topology optimizes implementation by placing the isolation amplifier (an inherently digital device) in a purely digital path and eliminates the need for DC-AC and AC-DC conversions of the analog error signal.

The advantages of this approach over traditional converter architectures are numerous. First, by eliminating the optocoupler (and its inherent CTR degradation issue), we have immediately improved the converter's reliability and long term operation. This is not a trivial result for space or military applications where 100% reliable operation in harsh environments is critical. Of special note is that this improvement in reliability does *not* come at the cost of additional components. On the contrary, eliminating the magnetics and chopper/rectifier circuits associated with the traditional high reliability magnetic coupling approach greatly reduces complexity and required board space of the final design. Another important advantage of the approach is that output voltage regulation tends to be superior relative to traditional feedback schemes. This is because the isolation barrier crossing has been relocated from the analog domain (error feedback path) to the digital domain (drive signal path). This reduces the number and type of components traversed by the error feedback signal which correspondingly reduces the injected offset and bias errors at this critical node. As a result of these simplifications, output voltage regulation is significantly improved.

The scheme does suffer from one important disadvantage, namely that the housekeeping supply design becomes slightly more complicated since an isolated output is now required to supply the PWM bias. One simple solution is to use a chopper-transformer-rectifier combination to bring an unregulated supply rail to the secondary side. Local regulation (e.g. linear or switching regulators) are then used to provide a stable regulated supply for the PWM. Note that this scheme is appropriate only for applications where the dynamic loads are small and the input voltage range is narrow. Other applications may need a more complicated design that could negate the benefits of using a secondary side referenced PWM in the first place.

To demonstrate the performance of the scheme shown in Fig. 13, a simple prototype converter was built and tested. The circuit was a basic flyback converter designed to supply 5 V output at several watts from an isolated 28 V input bus. Two separate benchtop power supplies were used to power input and output circuits in this demonstration. The returns of each supply were tied together at a single point at the input bench supply's chassis ground connection. Thus input and output circuits were galvanically isolated from each other with only the main power transformer and the isolation amplifier crossing the isolation barrier. The input voltage was allowed to vary from 22 V to 36 V while the output was loaded from 100 mA to 1A using variable resistors.

The results were exceptional in terms of both line and load regulation: less than 0.1% and 0.45%, respectively over the full operating range. These results are 2 to 3 times better than comparable designs employing traditional optical or magnetic coupling methods [17–19]. For completeness, we also performed a step load test to demonstrate the converter's transient response with the isolation amplifier in the feedback path. We would expect no discernable effect on dynamic performance since the amplifier faithfully transmits

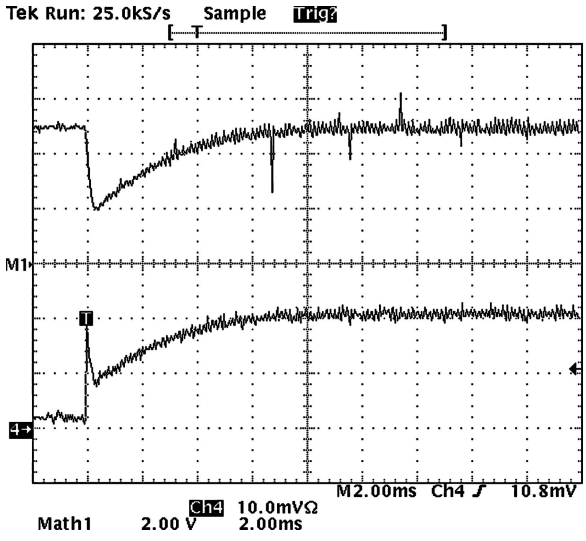

Fig. 14 Output voltage transient response (top trace) and load step stimulus (bottom trace)

the power pulses with negligible phase delay and therefore appears transparent to the control loop. Indeed this appeared to be the case as the stable, overdamped response in Fig. 14 demonstrates. In this scope plot, the load step current is the bottom trace at 500 mA/div and the output voltage transient response is the upper trace at 2 V/div. The load step was provided by momentarily switching a 5 Ω resistor in parallel with the nominal 50 Ω load. This resulted in a large current spike at the moment of switching as the output capacitance was quickly discharged. The input voltage in this test case was the minimum 22 V. We repeated the measurement at maximum input voltage of 36 V with similar results.

6. Summary

We designed and fabricated a 0.5 μm Silicon-on-Sapphire (SOS) 4-channel digital isolation amplifier to facilitate communication across the isolation barrier in galvanically isolated applications. The device has been demonstrated to operate in excess of 100 Mbps, rejects ground bounces of more than 5 V/μs with its differential transmission scheme, and provides more than 800 V of input-to-output isolation. The device effectively operates over the full military temperature range with little to no degradation in performance. The device offers significant improvements in reliability, size, and speed relative to existing optical and magnetic coupling schemes. We also demonstrated one important application of the amplifier in power conversion circuits. We showed how the isolation amplifier can replace optical and magnetic feedback methods to significantly improve design and performance of traditional power converter schemes. Test results of an isolated DC/DC converter employing the isolation amplifier to close the loop confirmed the performance improvement over several comparable traditional designs.

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