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A $3\,nV/\sqrt{Hz}$ rail-to-rail operational amplifier in silicon-on-sapphire with constant transconductance

Pujitha Weerakoon · Frederick J. Sigworth · Peter J. Kindlmann · Eugenio Culurciello

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Abstract This paper presents the design, fabrication, and electrical measurement results from a low-noise high-performance amplifier fabricated in the 0.5 μm silicon-on-sapphire (SOS) technology. The amplifier was designed with rail-to-rail input and output swing and constant transconductance in its entire common-mode range and targets biomedical instrumentation in SOS/SOI technologies. The amplifier reports $3\,nV/\sqrt{Hz}$ of input-referred voltage noise at 10 kHz and has 0.4 mV of input-referred offset. The gain-bandwidth product of the amplifier is 12 MHz and the open-loop gain is 75 dB. The amplifier occupies 0.08 mm^2 of area and consumes 1.4 mW of power.

Keywords Operational amplifiers · Rail-to-rail amplifiers · Silicon-on-sapphire · Low-noise amplifiers

1 Introduction

Recent developments in manufacturing have made SOS a feasible and much desired technology. SOS provides several advantages in mixed signal integrated circuit design over bulk CMOS technology. First, the absence of a conducting substrate significantly reduces parasitic capacitance and allows SOS devices to perform at much faster speeds than those made using conventional bulk CMOS technology [1, 2, 3, 4, 5, 6]. Second, the lower parasitic capacitance allows the fabrication of near-ideal passive elements such as resistors without any degradation in the frequency response [7, 8, 9]. Third, the non-conducting substrate also provides a means of isolating power supplies for digital and analog parts of a mixed-signal circuit yielding better noise performance. Fourth, the transparent sapphire substrate in SOS provides unique advantages in image sensor design [10].

The main contribution of this work is the design of a $3nV/\sqrt{Hz}$ operational amplifier with rail-to rail operation in the 0.5 μm silicon-on-sapphire process. Our design includes all the recent bulk CMOS techniques and advancements into an implementation in a SOI technology [11, 12, 13, 14]. This design is optimized for low-noise performance in SOS/SOI technologies and for use in biomedical instrumentation, and in particular for resistive head-stages in patch-clamp amplifiers [8]. In addition, our design features a new cascoded current differential amplifier circuit to provide constant transconductance for rail to rail operation of the amplifier. These innovations make this operational amplifier one of the lowest noise and high-performance SOS/SOI amplifiers for biomedical applications [15, 16]. Rail-to-rail amplification is desirable to best utilize the 3.3 V voltage range in the process and to increase the signal-to-noise ratio. Constant-transconductance of the operational amplifier is desirable in high-precision applications such as patch-clamp amplifiers where better than 0.1% linearity is needed [7].

This paper is organized as follows. In Sect. 2 we will present how we chose the device parameters and operating conditions for our design. In Sects. 3 and 4 we will present the design of the rail-to-rail, constant-transconductance input stage and the rail-to-rail output stage of the

P. Weerakoon · F. J. Sigworth · P. J. Kindlmann · E. Culurciello (✉)
School of Engineering and Applied Science, Yale University, New Haven, CT 06520, USA
e-mail: eugenio.culurciello@yale.edu

P. Weerakoon
e-mail: pujitha.weerakoon@yale.edu

operational amplifier, respectively. In Sect. 5 we will present how we compensated the amplifier. In Sect. 6 we will present the self-starting biasing circuit we designed to bias the operational amplifier. In Sect. 7 we will discuss the input-referred voltage noise of the operational amplifier. In Sect. 8 we will present the realization and the measurement results from the operational amplifier.

2 Device parameters and operating conditions for silicon-on-sapphire analog design

Table 1 shows the operating conditions and device parameters we chose for our design. We used a channel length of 5 μm, a $V_{DS,Sat}$ of 250 mV and a I_0 of 20 μA to obtain reasonable tradeoffs between speed, gain and output swing. The typical device widths for the NMOS and PMOS devices were chosen as 25 and 40 μm, respectively. In order to decide on typical device sizes for the design, SPICE models were used to simulate how I_o varies with V_{DS} for a channel length of 5 μm. The corresponding output resistances of both NMOS and PMOS devices were recorded. The simulation results are shown in Fig. 1a. The NMOS device, which has the highest level of doping, exhibits a kink at high V_{DS} values due to its floating substrate, which degrades the output resistance and thereby gain [17, 18, 19]. Although the output resistance can be increased by arbitrarily picking a higher channel length, this could make the device unacceptably slow.

Cascoding was used to increase the output resistance of devices [20]. When using this technique, the output swing is reduced due to the extra overdrive voltage needed across the cascode device which limits the output swing. However, cascoding is necessary to obtain reasonable output resistance in the SOS process. This is especially true when designing the input stage of operational amplifiers where high output resistance in current sources is vital for high common-mode rejection ratio (CMMR). Fig. 1b shows how cascoding the devices has increased the output resistance $R_{oN(cas)}$ and $R_{oP(cas)}$ of NMOS and PMOS devices to approximately 8 MΩ. The device sizes are the same as in the non-cascoded case. It is important to note here that the cascode output resistance is still much lower than that of a bulk CMOS process which is typically in the order of 10^9 Ω [21].

Table 1 Operating conditions and device parameters that will be used in the design

	NMOS	PMOS
Operating conditions		
Channel width/length, W/L (μm)	25/5	40/5
Gate to source voltage, V_{GS}	1.00 V	−0.900V
Bias current, I_0	20 μA	20 μA
Overdrive voltage, $V_{DS,Sat}$	0.250 V	−0.250 V
Device parameters		
Threshold voltage, V_{TH}	0.750 V	0.650V
Transconducrance parameter, K_T	150 μA/V^2	90 μA/V^2
Small signal transconductance, g_m	160 μA/V	160 μA/V
Output resistance, r_o	1 MΩ	1.5 MΩ
Cascoded output resistance, $R_{o(cas)}$	8 MΩ	8 MΩ
Gate oxide capacitance, C_{ox}	3.6 fF/μm^2	3.6 fF/μm^2
Flicker noise parameter, K_f	10^{-24}V^{2}F	10^{-24}V^{2}F

3 Constant transconductance rail-to-rail input stage

The folded-cascode amplifier based on two complementary NMOS, PMOS differential pairs shown in Fig. 2 can be used to get rail-to-rail performance from the input stage [21, 22]. The simulated variation of the total transconductance g_m over the input common-mode range of the folded-cascode stage is shown by the dashed line in Fig. 3. The transconductance g_m varies by a factor of two over the common-mode range depending upon whether one or both differential pairs are on [21]. This variation in transconductance leads to a variation in the gain-bandwidth product of the amplifier, when assuming an infinitely high DC gain and a single pole operational amplifier [23]. Furthermore, as we will discuss later, the capacitor used to compensate the amplifier is inversely proportional to the transconductance of the amplifier [20]. Therefore, the variations in the transconductance makes frequency compensation of the amplifier more difficult.

3.1 Adding two complementary current differential amplifiers to obtain constant transconductance

As seen from Table 1, typical device sizes were chosen so that transconductance (g_m) of the NMOS and PMOS devices are equal. Since the transconductance of one differential pair can be written as

$$g_m = \sqrt{2K_T\frac{W}{L}I_0} \tag{1}$$

a constant transconductance G_m given by

$$G_m = 2\sqrt{2K_T\frac{W}{L}I_0} = 2g_m \tag{2}$$

can be achieved over the whole input common-mode range by adding a current of $3I_0$ to the active differential pair when the complementary differential pair is off [21, 22]. This can be done by integrating NMOS and PMOS based cascoded current differential amplifiers (CCDAs) with gains of $K1$ and $K2$, respectively, to the folded-cascode input stage as shown in Fig. 4.

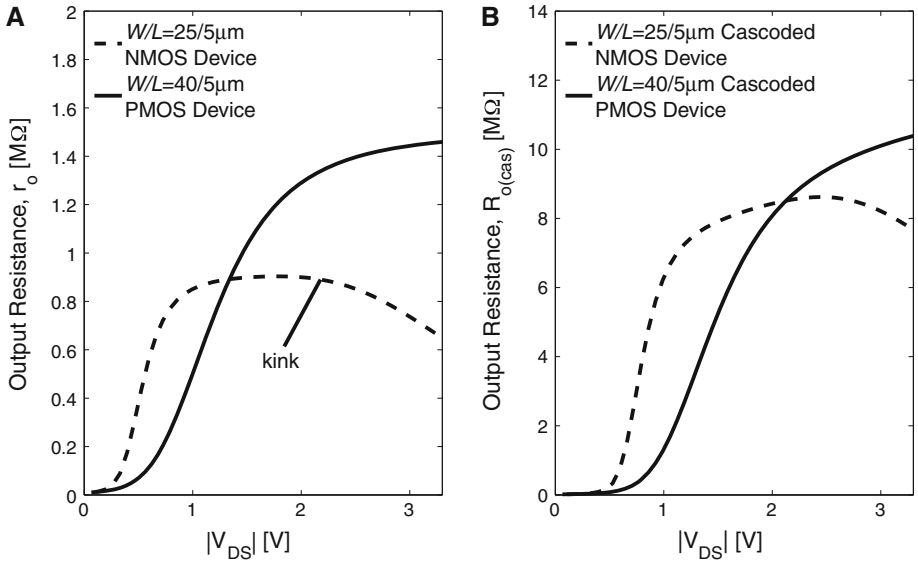

Fig. 1 Cascoding increases the output resistance of the devices. The *W/L* ratios of the NMOS and PMOS devices were 40/5 and 25/5 µm, respectively

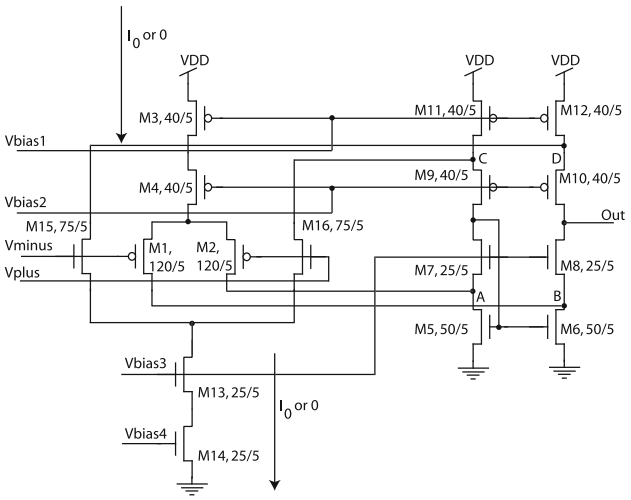

Fig. 2 A folded-cascode amplifier based on two complementary PMOS and NMOS differential pairs that has rail-to-rail input common-mode range. However, due to variable transconductance this amplifier is difficult to compensate over the common-mode range and suffers from non-linearity

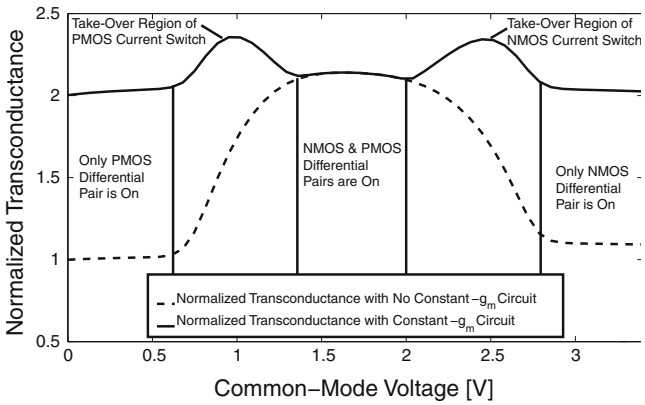

Fig. 3 The simulated normalized transconductance (g_m) variation of the amplifier with and without the constant g_m circuit. Without the constant g_m circuit, the transconductance varies by a factor of two over the input common-mode range. With the constant g_m circuit, the transconductance variation is approximately constant over the input common-mode range except at the take-over regions of the current switches where g_m varies by approximately 15%

Figure 5 shows the architecture of the NMOS CCDA with gain K used in our design. Cascoding was used to increase the gain of the amplifiers. When $i_1 = i_2 = 0$, a current of I_0 flows through all MOSFETs. If i_1 at node A increases to some value above zero but less than I_0, then i_{d3} increases by i_1. This increase in drain current is mirrored in i_{d4} with a gain of K since M4T, M4B are K times wider than M3T and M3B causing the amplifier to sink a current of Ki_1. A similar argument can be used to show that an increase in i_2 would make the amplifier source a current of Ki_2. Therefore, the current that the CCDA sinks at the output is given by

$$i_{\text{sink}} = K(i_1 - i_2) \tag{3}$$

Here we have discussed a NMOS based CCDA. The architecture of the PMOS based CCDA is symmetrically identical.

The operation of the constant-transconductance input stage in Fig. 4 can be understood thus: The MOSFETs MS1, MS2 and MS3, MS4 act as PMOS and NMOS current switches, respectively. When both differential pairs are on, the current sunk by both CCDAs is zero. This is because both node A and node B in each CCDA are connected to a current of I_0 and the difference is zero. Now, if the input common mode-voltage becomes high enough to shut down the PMOS differential pair, it also shuts down the PMOS current switch formed by MS1 and MS2 causing the NMOS CCDA to sink a current of $K1I_0$. This current is added to the NMOS differential pair increasing transconductance. The behavior at

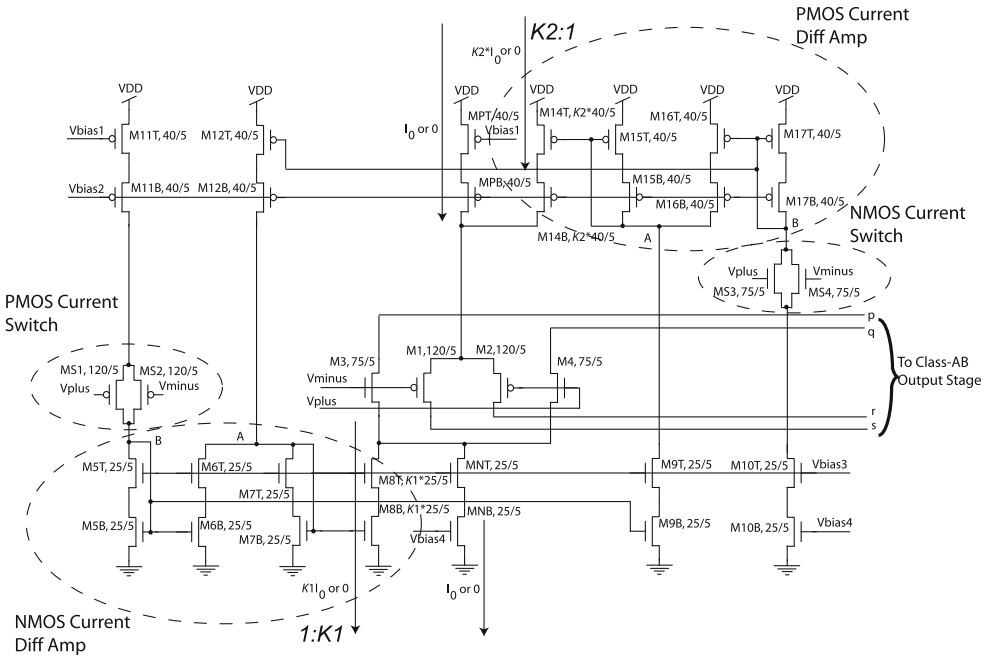

Fig. 4 The architecture of the Constant-transconductance input stage. Constant-transconductance was achieved by integrating two complementary CCDAs (*circled*) along with two current switches into the rail-to-rail input stage. Bias voltages Vbias1–4 were applied using the integrated biasing circuit described in Sect. 6

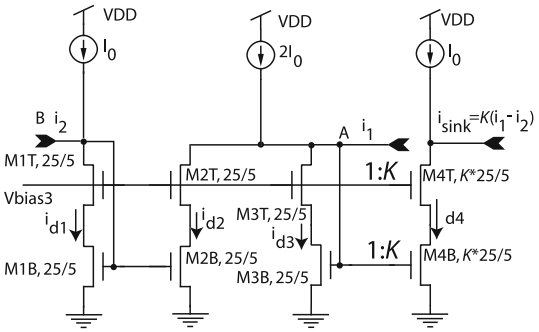

Fig. 5 A cascoded current differential amplifier (CCDA) with a gain of K

low common-mode voltages is symmetrically identical. We used a NMOS and PMOS CCDAs with gain $K1 = 6$ and $K2 = 5$, respectively, to implement the constant-transconductance circuit. The solid line in Fig. 3 shows the simulated normalized transconductance (g_m) variation of the amplifier with the constant-g_m circuit. The transconductance is approximately constant over the whole input common-mode range except at the take-over regions of the current switches where g_m varies by approximately 15%. We scaled the widths of the input transistors of both the NMOS and PMOS differential pairs to be three times the typical values shown in Table 1 to increase the gain of the input stage [20].

4 Rail-to-rail, push–pull, output stage

One design goal for out operational amplifier was to drive a 10 nF capacitive load so that it can be used in conjunction with a high-performance sigma–delta analog-to-digital converter (ex:-AD73360 from Analog Devices). In our design, we used a class-AB push–pull output stage with large current drive and low quiescent power dissipation [21]. The output stage has a topology like that of an inverter and allows the output to swing from rail-to-rail. The push–pull stage was integrated into the operational amplifier as shown in Fig. 6. The floating current sources MFCN1 and MFCP2 were used to precisely set biases in the output stage. A discussion on floating current sources can be found in [21, 22]. The floating current sources MFCN2 and MFCP2 were added to equalize the voltage across M20 and M21 and also across M22 and M23 to improve matching. The small signal gain A_{PP} of the push–pull amplifier is given by

$$A_{PP} = (g_{mon} + g_{mop})R_L||r_{on}||r_{op} \quad (4)$$

where g_{mon} and g_{mop} are the small signal transconductances and r_{on} and r_{op} are the output resistances of MON and MOP, respectively. R_L is the load resistance.

Since the transconductance of MON and MOP increases with the square root of the bias currents, we have sized MOP and MON to have ten times the quiescent current of the folded cascode stage to increase gain [21]. The push–pull amplifier's current drive can be considerably larger than the quiescent current due to its class-AB action [20]. Figure 7 shows the response of the operational amplifier to ±5 mV variation at the input with a 15 kΩ load connected to push–pull stage's output. In (A) we see that the output offset was only a fraction of a millivolt and that the amplifier can swing rail-to-rail. In (B) the low frequency

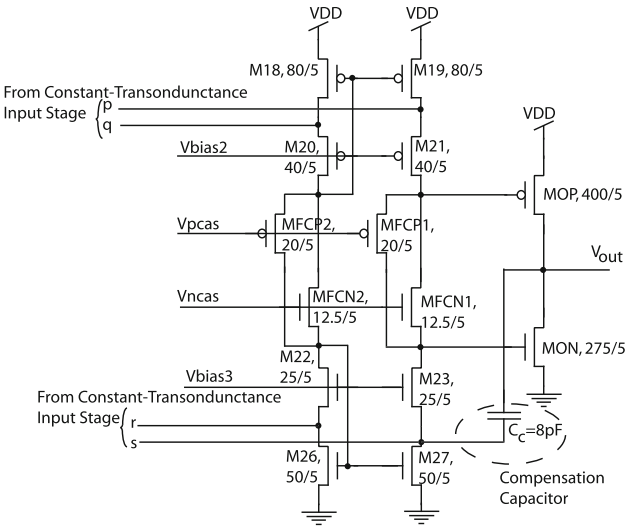

Fig. 6 A class-AB push–pull amplifier was added to the amplifier for higher speed and more output swing. The push–pull stage was biased using floating current sources labeled in the figure. A compensation capacitance C_c of 8pF was used to design the amplifier for a gain-bandwidth product of 10 MHz. Biases Vbias2–3, Vpcas and Vncas were provided using an integrated biasing circuit

gain of the operational amplifier was calculated as 5000 (75 dB) by taking the derivative of the curve shown in (A).

5 Compensating the operational amplifier

The operational amplifier was compensated using the Miller technique using a compensation capacitance of C_c as shown in Fig. 6 [21, 22]. The value of C_c that would result in a gain-bandwidth of f_c in the absence of other poles can be written as

$$C_c = \frac{G_m}{2\pi f_c} \tag{5}$$

where G_m is the constant transconductance of the input stage. Using Table 1, $G_m = 2g_{mn}\sqrt{3} = 544\,\frac{\mu A}{V}$. We designed our amplifier to have a gain bandwidth of 10 MHz and chose C_c to be 8 pF. Figure 8 shows the simulated loop gain of the operational amplifier when being driven as a voltage follower with a load resistance of 15 kΩ. The operational amplifier was unity-gain stable with a phase margin of 50°. The low frequency gain was 75 dB in agreement with Fig. 7b.

6 Biasing the operational amplifier

A beta-multiplier based biasing network was designed to provide the biases Vbias1–4, Vncas and Vpcas used by the operational amplifier [24]. A self-start circuit was included to assure that the biasing network snaps to the correct state [21]. The typical sizes for the biasing circuit were chosen to be the same as those for the operational amplifier so that the operating conditions in Table 1 are met. A discussion on beta-multiplier based biased circuit design can be found in [21].

7 Input-referred voltage noise of the operational amplifier

The input referred voltage noise (V_n) variation with frequency f of the operational amplifier can be calculated as

$$V_n(f) = \frac{32k_{BT}}{3g_m} + \frac{2}{C_{oxf}}\left(\frac{K_{fn}}{W_nL_n} + \frac{K_{fp}}{W_pL_p}\right). \tag{6}$$

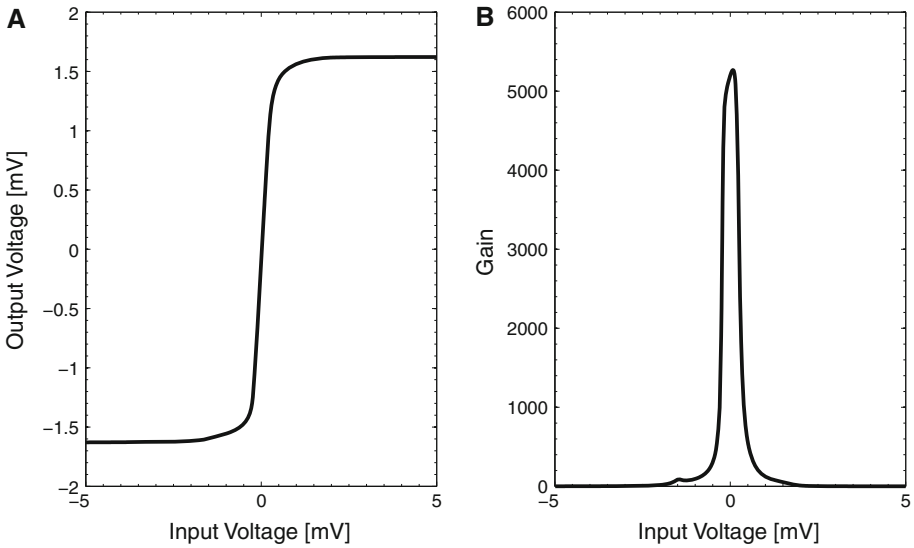

Fig. 7 **a** The simulated response of the operational amplifier to a ±5 mV signal at the input with a 15 kΩ load connected to push–pull stage's output. The input-referred offset was a fraction of a millivolt and the amplifier was able to swing rail-to-rail. **b** The low frequency gain of the operational amplifier was calculated as 5000 (75 dB) by taking the derivative of the curve shown in (**a**)

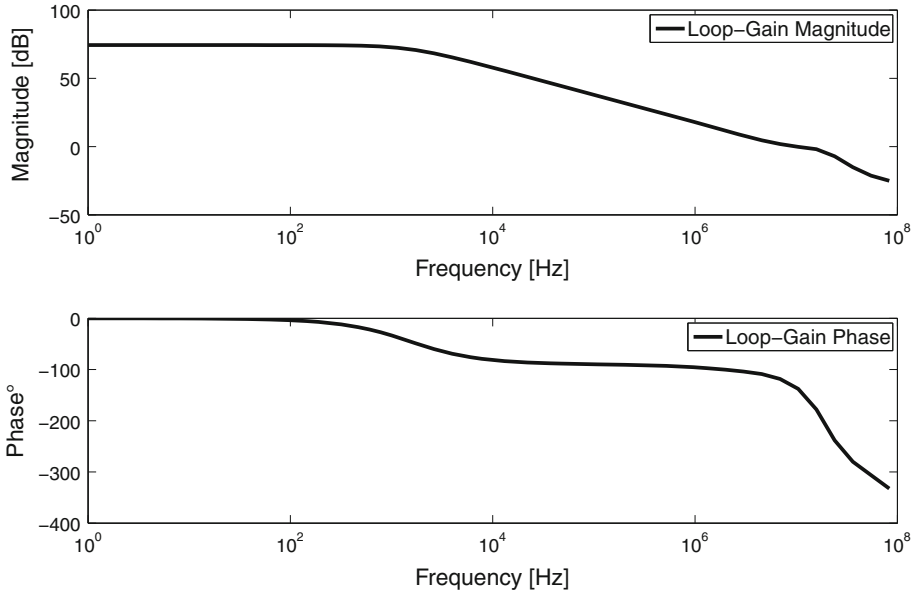

Fig. 8 The loop gain of the operational amplifier when being driven as a unity gain follower with a C_c of 8 pF and a load resistance of 15 kΩ. The operational amplifier is unity gain stable with a phase margin of 50°

Here, k_B is the Boltzman's constant of 1.38×10^{-23}J/K. K_{fn} and K_{fp} are the flicker noise coefficients for silicon-on-sapphire NMOS and PMOS devices, respectively [20, 21, 25]. T is the absolute temperature and C_{ox} is the gate oxide capacitance per unit area. W_n, L_n and W_p, L_p are dimensions of the input transistors in the NMOS differential pair and PMOS differential pair respectively. The values of K_{fn}, K_{fp}, and C_{ox} are given in Table 1 (Fig. 9).

8 Measurement results from the operational amplifier

The operational amplifier was designed in silicon-on-sapphire technology using Peregrine semiconductor's 0.5 µm CMOS process [26]. The die micrograph of the fabricated operational amplifier is shown in Fig. 10. The operational amplifier occupies an area of 400 µm × 180 µm. We have tested five different devices without noticing any statistical difference in performance between them. Monte Carlo analysis was not possible for lack of models. We here report the resulting typical performance data.

Figure 11 shows the measured and theoretical open-loop gain of operational amplifier with a load resistance (R_L) of 15 kΩ. Figure 12 shows the gain-bandwidth product variation of the amplifier with input common-mode voltage. The gain-bandwidth product was about 12 MHz over the entire input common-mode range. It is of interest to note here that constant gain-bandwidth product over the input common-mode range also implies constant-transconductance [21] .

Figure 13 shows the input-referred offset (V_{os}) variation of the amplifier with common-mode voltage (V_{cm}). The input referred offset was about 0.4 mV at zero common-mode voltage and about 4.5 mV at the rails. Figure 14 shows the response of the operational amplifier when configured as a voltage follower and when driven by 1 kHz sine wave with rail-to-rail input swing. The load at the amplifier's output was 15 kΩ. The amplifier was able to follow the input correctly and thus demonstrate its rail-to-rail input-output capability.

Figure 15 shows the measured input-referred voltage noise compared with the theoretical noise of the amplifier.

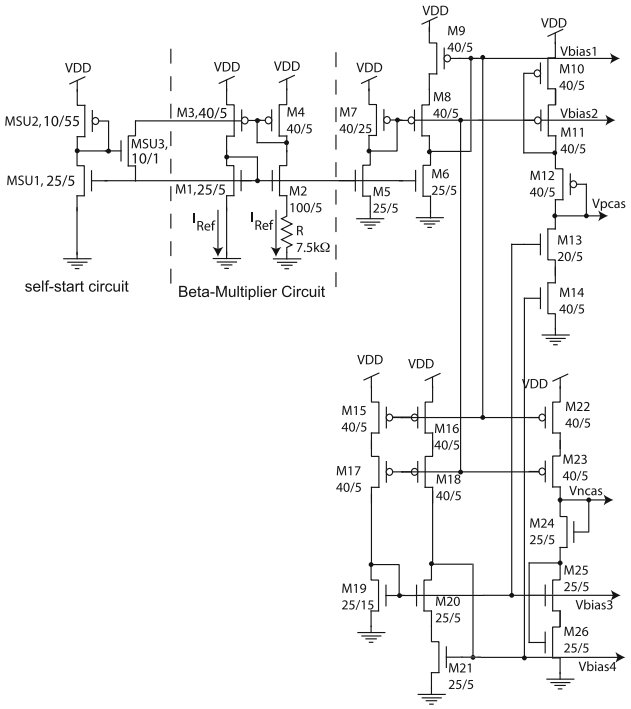

Fig. 9 A beta-multiplier based, self-starting biasing network was designed to bias the operational amplifier

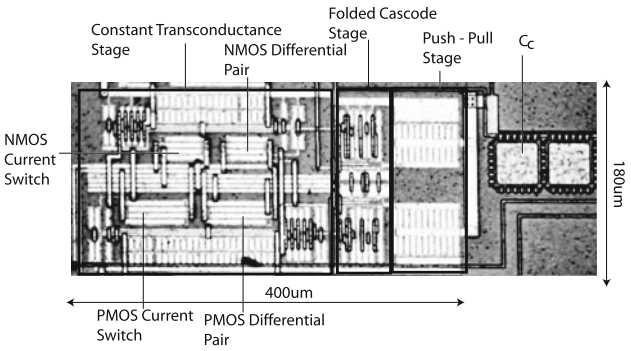

Fig. 10 The die micrograph of the fabricated operational amplifier. The operational amplifier occupied an area of 400 μm × 180 μm

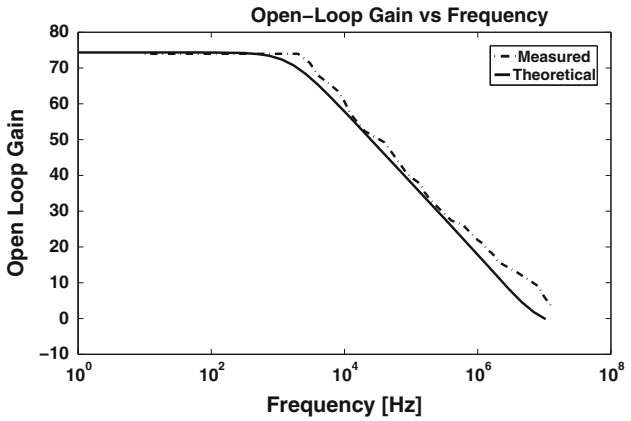

Fig. 11 The measured and theoretical open-loop gain of the operational amplifier with a R_L of 15 kΩ. The low frequency gain was 75 dB and the unity-gain frequency was 12 MHz

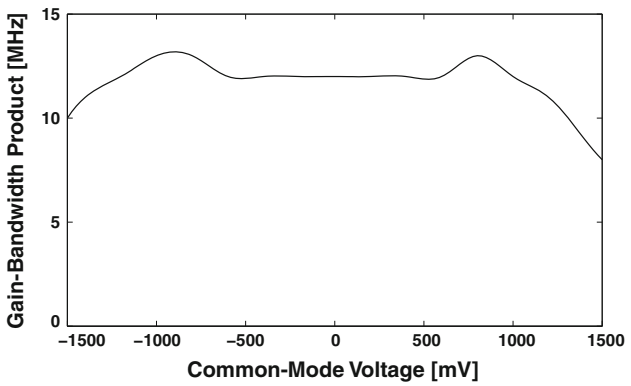

Fig. 12 The gain-bandwidth product variation of the operational amplifier over the input common-mode range. The gain-bandwidth product was 12 MHz over the entire input common-mode range

The voltage noise of the amplifier was approximately $9 \times 10^{-18}\ \frac{V^2}{Hz}$ or $3 \times 10^{-9}\ \frac{V}{\sqrt{Hz}}$ at 10 kHz (Table 2). This is the lowest noise reported for an SOS/SOI design and currently a reference design for biomedical instrumentation implemented in SOS/SOI. This design is also an enabling technology for resistive head-stages in patch-clamp amplifiers [8] II gives a summary of the measurement results for the operational amplifier and shows how we were able to meet all design goals.

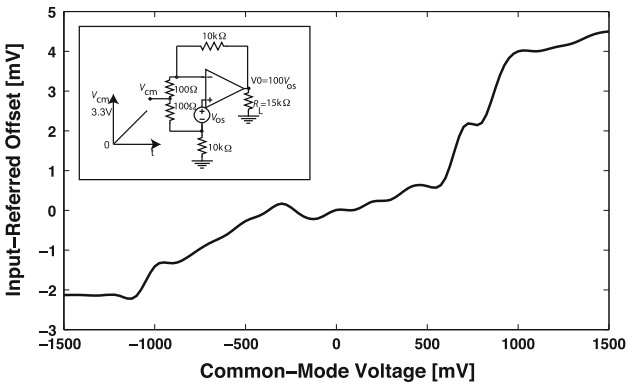

Fig. 13 The measured input-referred offset (V_{os}) variation with common-mode voltage (V_{cm}). Configuration of operational amplifier to measure the input-referred offset (*inset*)

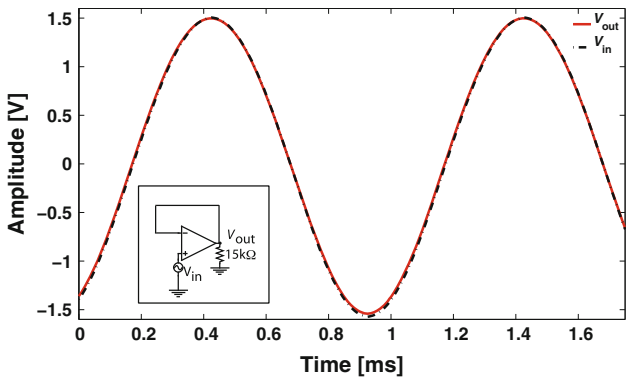

Fig. 14 Measured response of the operational amplifier when configured as a voltage follower and when driven by 1 kHz sine wave with rail-to-rail input swing. The amplifier was able to follow the input correctly and thus demonstrate its rail-to-rail input-output capability. The load at the amplifier's output was 15 kΩ

9 Summary

This paper presents the design, fabrication and test results from a low-noise rail-to-rail, constant-transconductance, operational amplifier made using silicon-on-sapphire technology. The amplifier reported a low noise figure of $3nV/\sqrt{Hz}$, a gain-bandwidth product of 12 MHz and occupies an area of just 0.08 mm^2. This high-performance is amplifier can act as a building block for biomedical instrumentation in the silicon-on-sapphire technology.

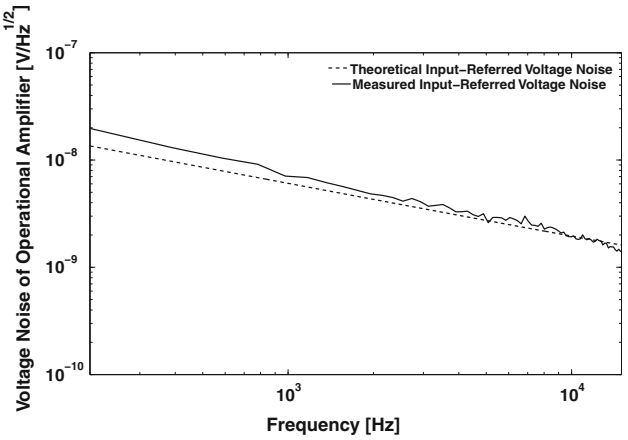

Fig. 15 The measured and theoretical input-referred voltage noise of the amplifier. The voltage noise of the amplifier was about $3 \times 10^{-9} \frac{V}{\sqrt{\text{Hz}}}$ or about $9 \times 10^{-18} \frac{V^2}{\text{Hz}}$ at 10 kHz

Table 2 Measurement results for operational amplifier

Parameter	Expected	Measured
Die area		0.08 mm^2
Open loop gain	75 dB	75 dB
Gain-bandwidth product	10 MHz	12 MHz
Constant-transconductance? (gain-bandwidth)	Yes	Yes
Input-referred offset voltage	<1 mV	0.4 mV
Input common-mode range	0–3.3	0–3.3 V
Output swing	0–3.3	0–3.3 V
Slew rate	$8 \frac{\text{V}}{\mu s}$	$10 \frac{\text{V}}{\mu s}$
Input-referred voltage noise at 10kHz	$3 \times 10^{-9} \frac{\text{V}}{\sqrt{\text{Hz}}}$	$3 \times 10^{-9} \frac{\text{V}}{\sqrt{\text{Hz}}}$
Quiescent current	400 μA	430 μA
Input capacitance	2.3 pF	2.6 pF

$R_L = 15\,\text{k}\Omega$, VDD=3.3V

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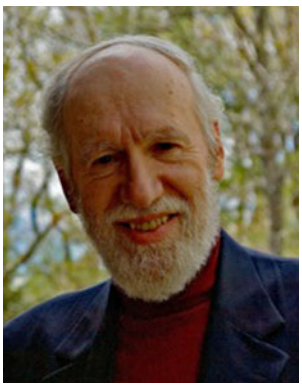
Pujitha Weerakoon received the BSE Degree in Electrical and Computer Engineering from Lafayette College, Easton, PA, in 2004 and the MS and M.Phil Degrees in Biomedical Engineering from Yale University in 2006 and 2007, respectively. He obtained his PhD in Biomedical Engineering in the laboratory of Fred Sigworth and Eugenio Culurciello in 2009. In 2009 he was a postdoctorate associate for prof. Fred Sigworth. He is interested in the design of mixed signal integrated circuits for biomedical and sensing applications.

Fred J. Sigworth received the B.S. degree in applied physics from California Institute of Technology, Pasadena, and the Ph. D. degree in physiology from Yale University, New Haven, CT, where he worked in the laboratory of C. F. Stevens. He was a Postdoctoral Fellow in the laboratory of E. Neher in Göttingen. Since 1984, he has been a Faculty Member in the Department of Cellular and Molecular Physiology at the Yale School of Medicine, and holds a joint appointment in the Department of Biomedical Engineering. His research group studies the function and structure of ion-channel proteins.



Peter J. Kindlmann is Professor (Adjunct) of Electrical Engineering at Yale University. He received the B.S. degree in Physics from Columbia University in 1962 and the M.S. in Physics and Ph.D. degrees in Engineering and Applied Science from Yale University in 1963 and 1966. At Yale since 1966, he was the founder and director of Yale's Instrumentation Lab, the first university-wide laboratory for the design of research instrumentation for the physical, biological and medical sciences (1965-79). He has won several teaching awards at Yale, and collaborated and published in research in robotics, laser physics, computer engineering, biomedical engineering and medicine. He now divides his time between Yale and his consulting practice in the field of instrumentation and product design. Current such interests include high-performance quadrupole mass spectrometry, biotechnology, custom sensors for industrial and medical applications, and occasional work in consumer electronics. He is a Life Senior Member of the IEEE and the inventor or co-inventor of 20 patents.

Eugenio Culurciello received the Laurea (M.S.) degree in Electronics Engineering from the University of Trieste, Italy, in July 1997. His MS thesis work was developed at Johns Hopkins University with professor Ernst Niebur. He joined professor Andreas G. Andreou laboratory in January 1998 as a graduate student. He received a second M.S. degree in Electrical and Computer Engineering from Johns Hopkins University, Baltimore. In September 2004 he received the Ph. D. degree in Electrical Engineering at The Johns Hopkins University. In July of 2004, Mr. Culurciello joined the Department of Electrical and Computer Engineering at Yale University where he currently is an associate professor and directs Yale's 'e-Lab', a VLSI laboratory. His research aims at extending the performance of CMOS circuits by means of advanced VLSI technologies. He focuses on topologies and circuits that take advantage of the native properties of devices to augment their computational and communication capabilities. His research interests originate from the identification of the physical limitations of current integrated circuits technologies. These limitations suggest efficient algorithms to encode information in ways that are compatible with the physical medium where computation and communication is performed. His research interests include: analog and mixed-mode integrated circuits with applications to biomedical instrumentation, biological sensors and interfaces, implantable sensors, telemetry sensors, biomimetic sensors. Bio-inspired vision sensory systems and application in Sensor Networks, efficient communication systems, event-based communication and processing. Silicon on Insulator and Silicon on Sapphire circuit design, models of devices, analog-to-digital conversion, radio circuits, radiation tolerant design and isolation amplifiers. He is the author of the book "Silicon-on-Sapphire Circuits and Systems, Sensor and Biosensor interfaces" published by McGraw Hill in 2009.